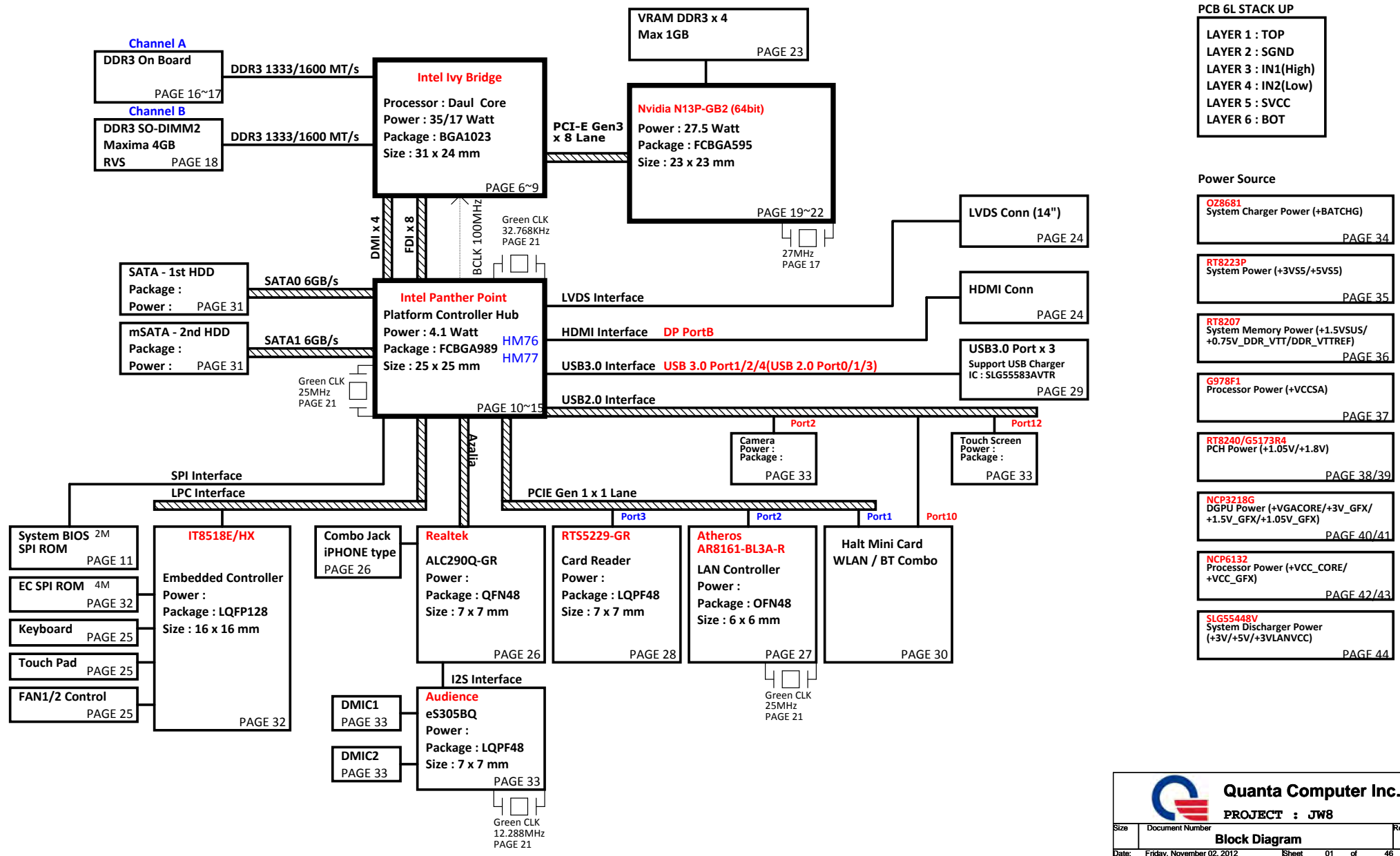
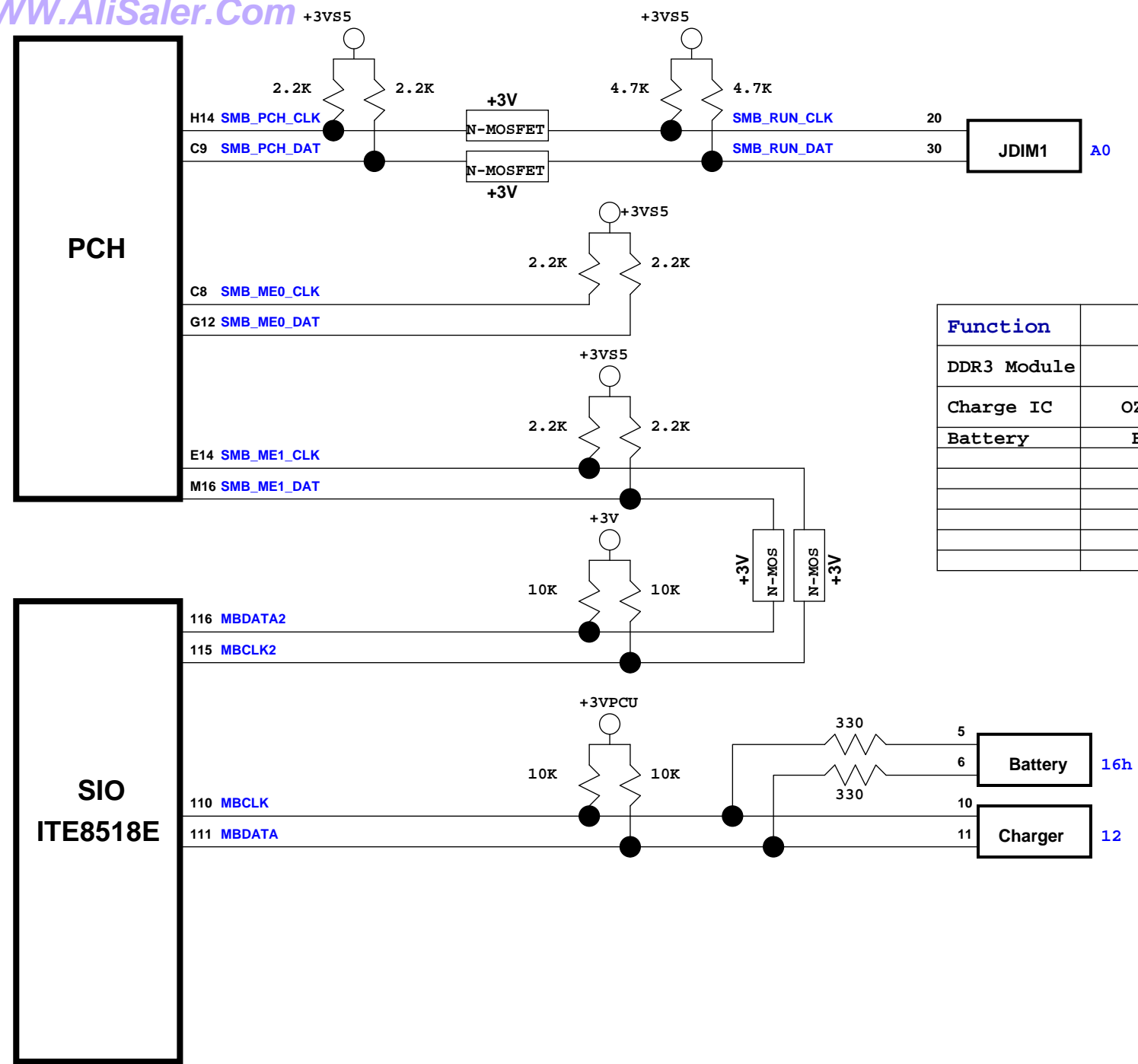


JW8 DIS (14") Super Ultra

Intel Chief River Platform Block Diagram





Function	IC	SMBus Address
DDR3 Module	JDIM1	A0h
Charge IC	OZ8681NL	0b0001001x (0x12h)
Battery	Battery	16h

USB Master	Port Assignment
USB0	External port#1 (USB3.0)
USB1	External port#2 (USB3.0)
USB2	Camera
USB3	External port#3 (USB3.0)
USB4	NC
USB5	NC
USB6	NC
USB7	NC
USB8	NC
USB9	Debug
USB10	WLAN
USB11	NC
USB12	Touch Screen
USB13	NC

SATA Master	Port Assignment
SATA0	HDD
SATA1	mSATA
SATA2	NC
SATA3	NC
SATA4	NC
SATA5	NC

PCIE Master	Port Assignment
PCIE 1	WLAN
PCIE 2	LAN
PCIE 3	Card reader
PCIE 4	NC
PCIE 5	NC
PCIE 6	NC
PCIE 7	NC
PCIE 8	NC

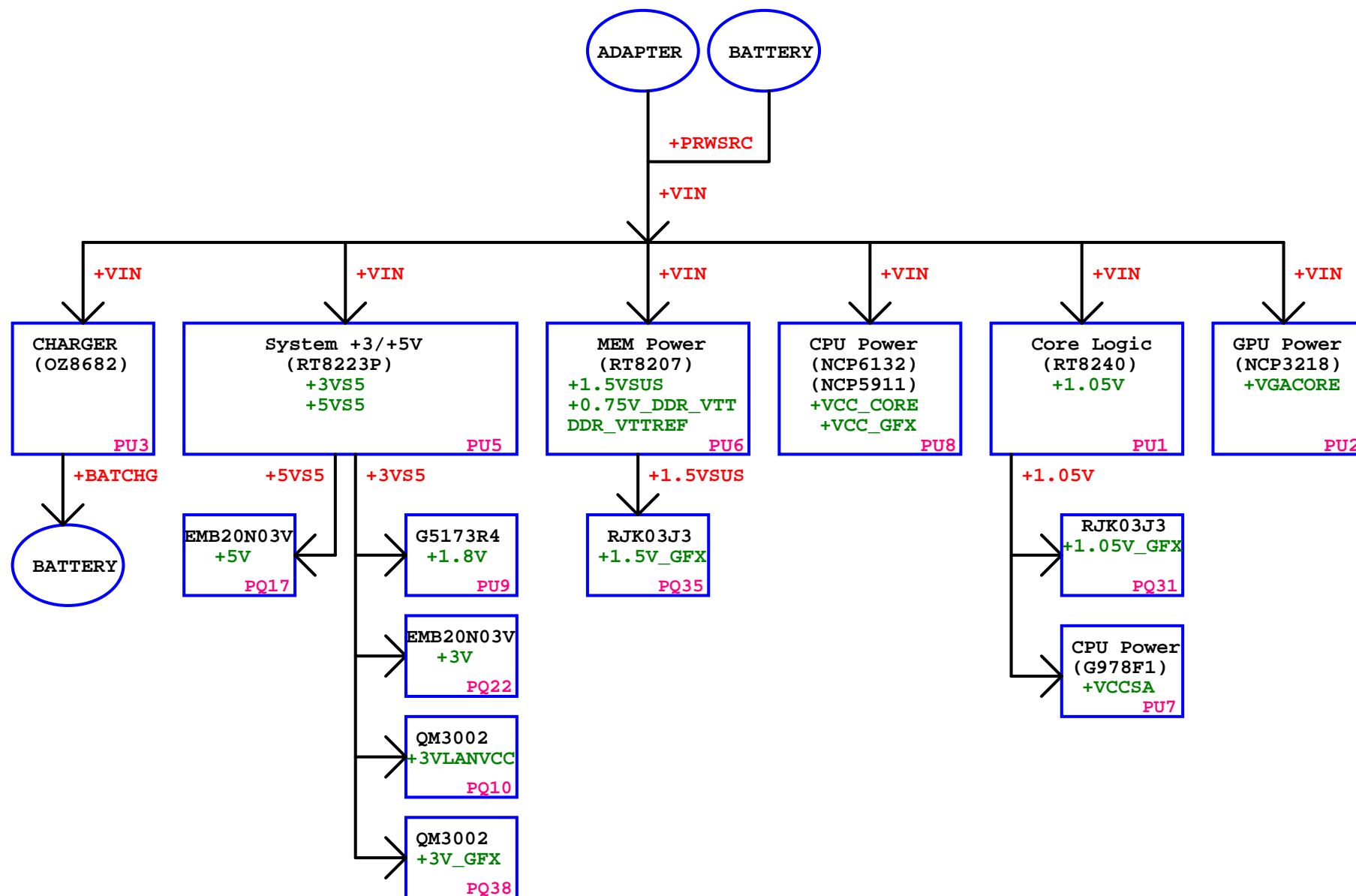


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PROJECT : JW8

Size	Document Number	Rev
	PORT ASSIGNMENT	3A
Date:	Friday, November 02, 2012	Sheet 03 of 46

Main Power tree



Chief River mainly Power On Sequence(G3 to S0)

From Coin Cell BAT

VCCRTC

From AC,BATT

VIN

Sys +3v/+5v VR internal power

+5VPCU/ +3VPCU

From PW On Button to EC

NBSWON#

EC Assert S5_On when received NBSWON#

S5_ON

From EC(S5_ON) to System +3V/+5V PWM

+3VS5/+5VS5

From EC to PCH

EC_RSMRST#

From EC to PCH

DNBSWON#

PCH assert SUSCLK

SUSCLK

SUSCLK RUNNING

From PCH to EC

SUSB#/SUSC#

PCH Asserted SUSB#/SUSC# to EC to assert SUSON..

EC Assert SUS_ON

SUS_ON

SUSON Power rail

+1.5VSUS

EC Assert LAN_POWERON

LAN_POWERON

EC Assert MAIN_ON

MAIN_ON

MainOn Power Rails

+3V/+5V/+1.05V/+1.8V/+1.05V_VTT

1.05V_VTT_PWRGD to enable +VCCSA

1.05V_VTT_PWRGD

EC Received HW_PG
from MainOn/SUSON/VCCSA PowerGD

HW_PG

EC Assert VR_ON

VR_ON

EC defined 105ms from HWPG to VRON

EC Assert EC_PWROK

EC_PWROK(PCH_PWROK)

EC defined 125ms from HWPG to ECPWROK

IMVP_PWRGD to PCH SYS_PWROK

IMVP_PWRGD(PCH_SYS_PWROK)

DRAMPWROK DRAMPWROK

PCH assert UNCOREPWRGOOD to CPU

H_POWERGD

PCH Assert PLTRST#

PLTRST#

DMI

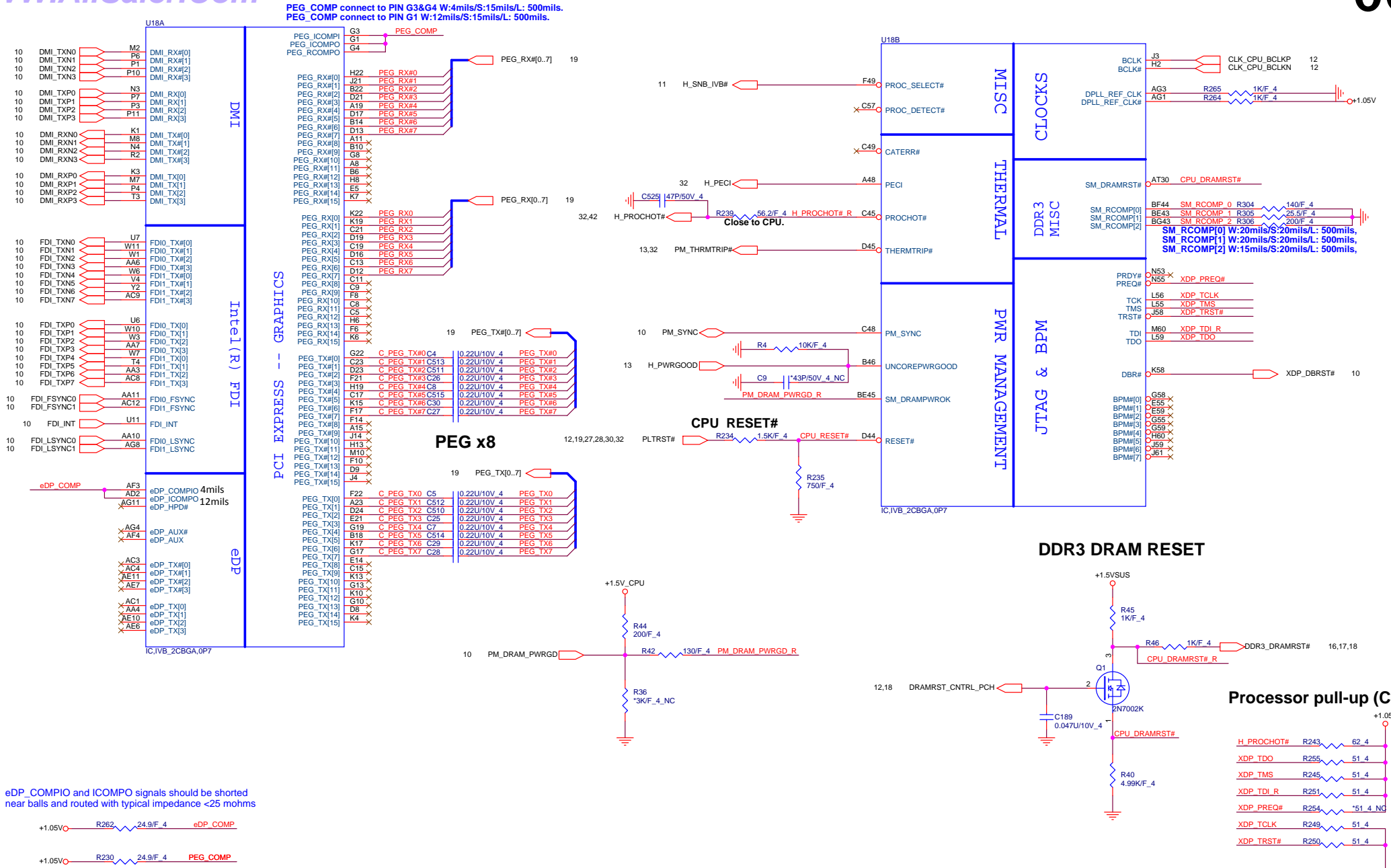
DMI_BUS



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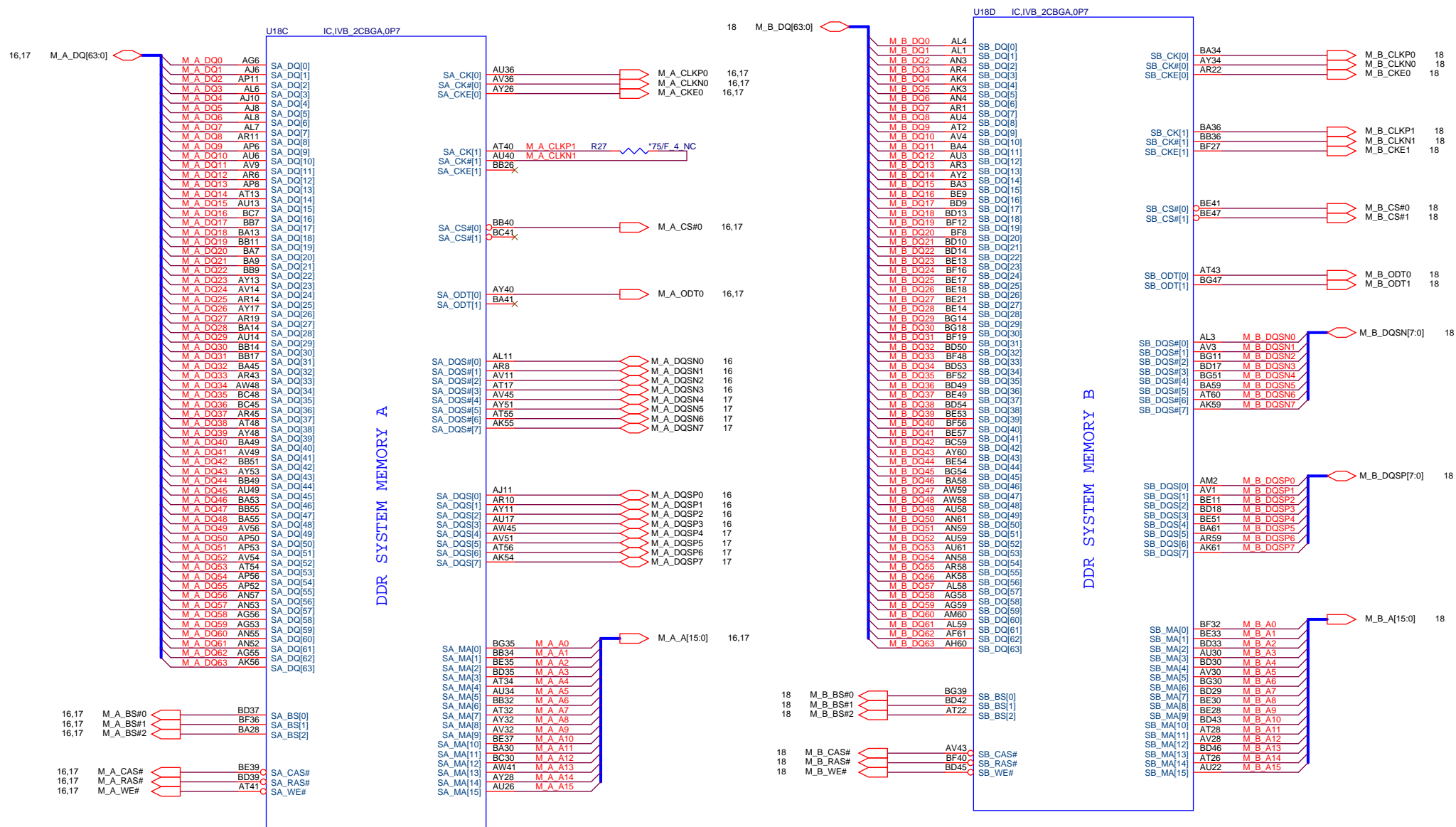
PROJECT : JW8

Size	Document Number	Rev
	Power On Sequence	3A
Date:	Friday, November 02, 2012	Sheet 05 of 46



Ivy Bridge Processor (DDR3)

07

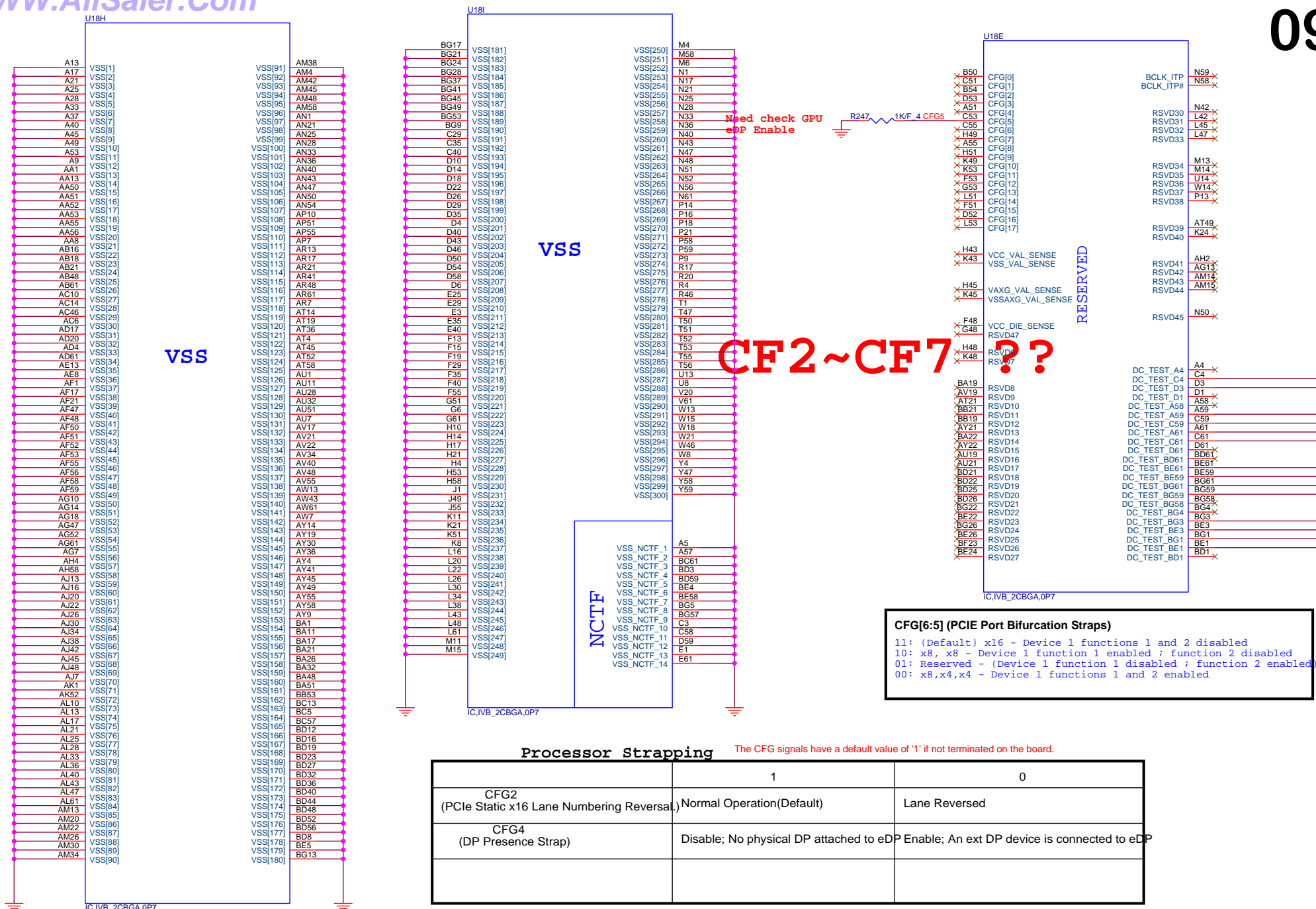


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PROJECT : JW8

Size	Document Number	Rev
	Processor 2/5 (DDR3 I/F)	3A
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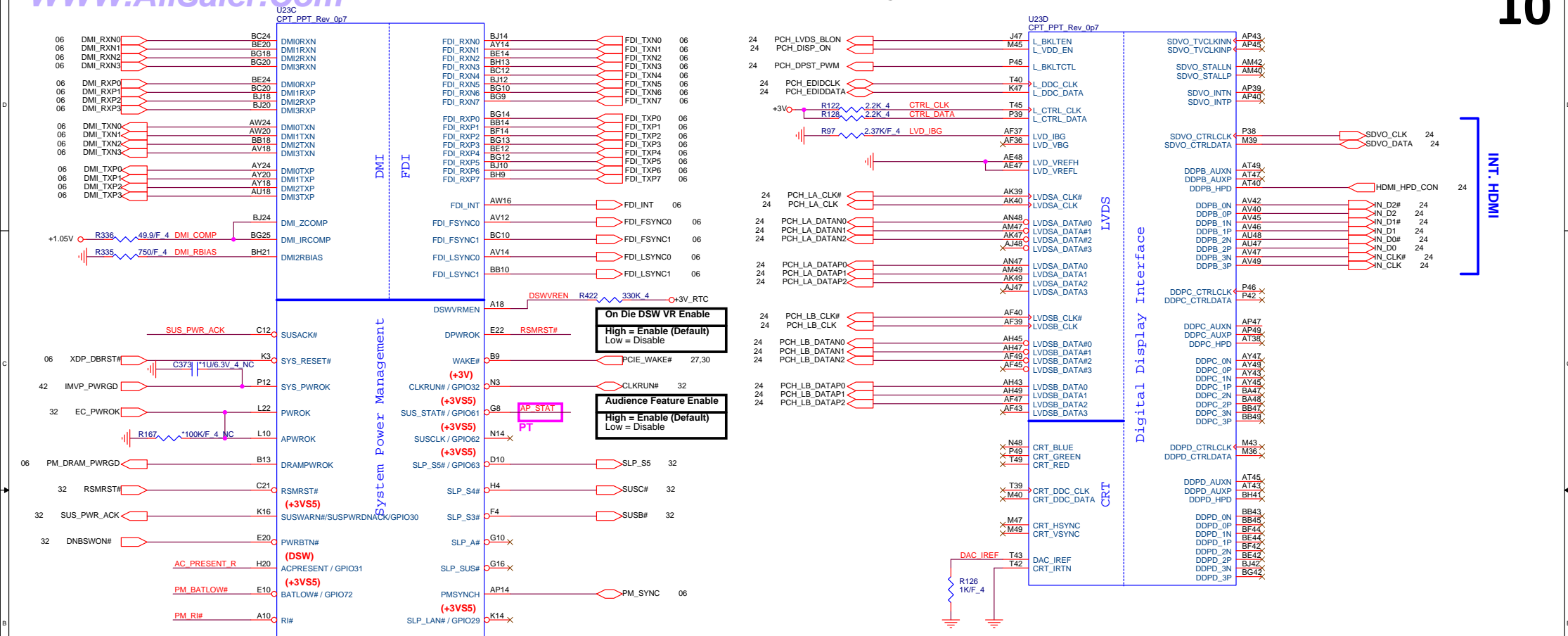




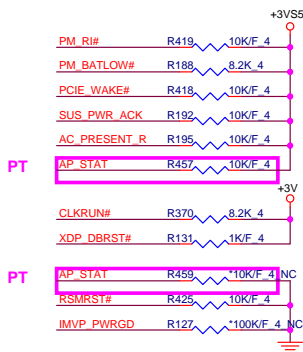
Quanta Computer Inc.

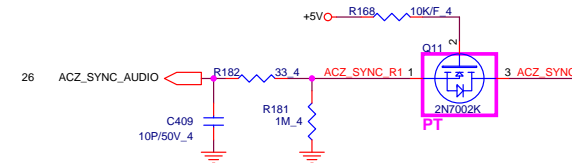
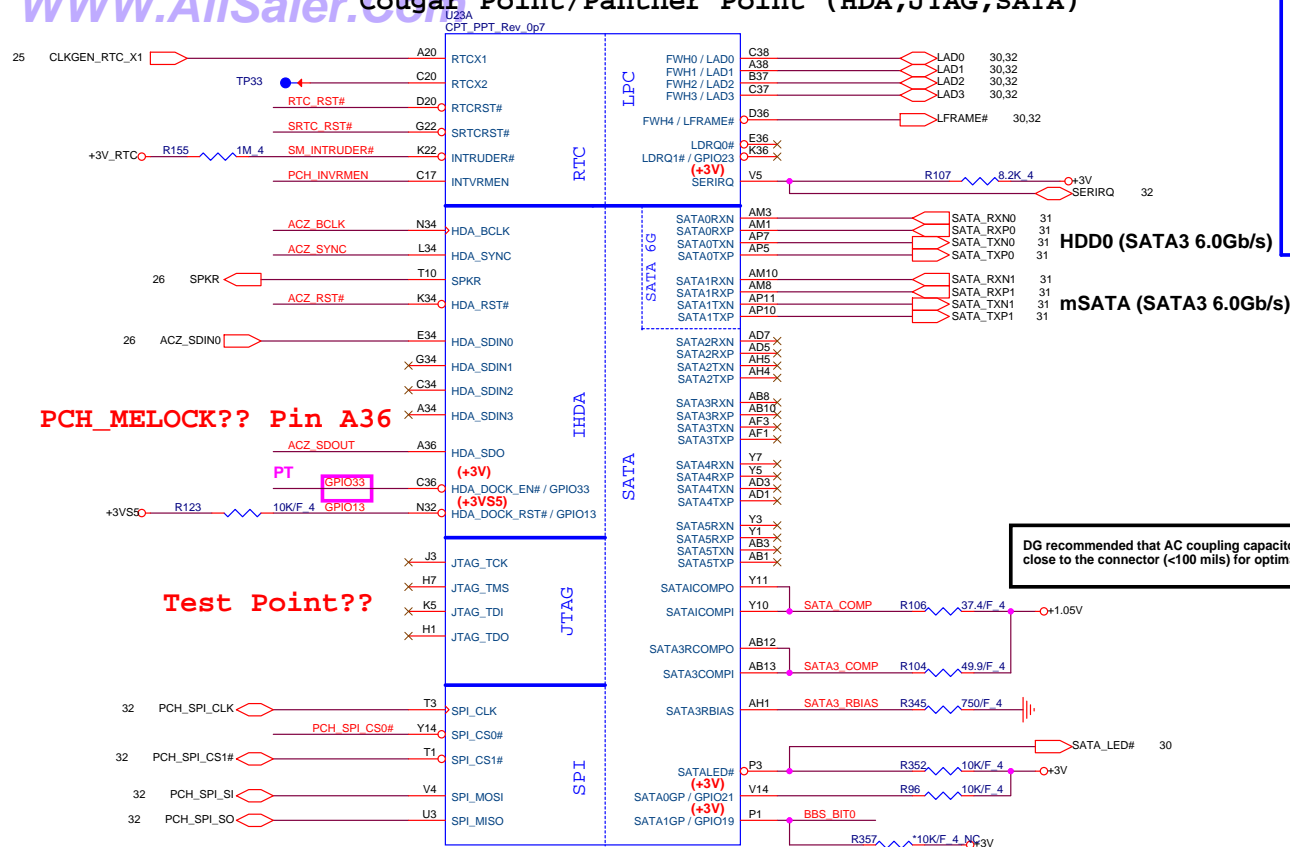
PROJECT : JW8

Processor 4/4 (RSV,Ground)

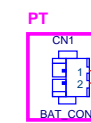


PCH Pull-high/low(CLG)



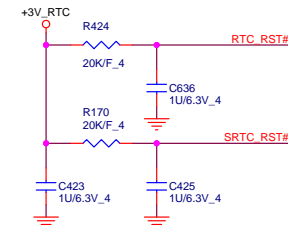


RTC Circuitry(RTC)

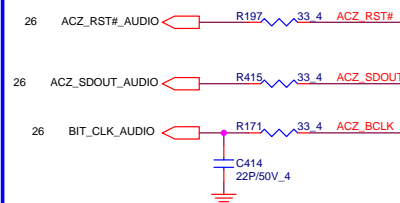


RTC Power trace width 20mils.

30mils

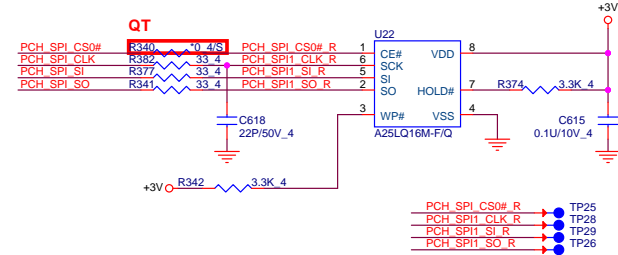


HDA Bus(CLG)



Vender	Size	P/N
AMIC	2MB	AKE38ZN0802 (A25LQ16M-F/Q)
GGD	2MB	AKE38GN0Q00 (GD25Q16BSIGR)

PCH SPI ROM(CLG)



PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	Circuit
SPKR	No reboot mode setting	PWR0K	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	
GNT3# / GPIO55	Top-Block Swap Override	PWR0K	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	+3V R387 10K/F_4 PCI_GNT3# 12
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+3V_RTC R423 330K 4 PCH_INVRMEN
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security Only for Interposer	PWR0K	0 = Override 1 = Default (weak pull-up 20K)	GPIO33 R444 *1K/F_4 NC ACZ_SDOUT 32 PT
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWR0K	[Need external pull-down for LPC BIOS] Default weak pull-up on GNT0/1#	
GPIO19	Boot BIOS Selection 0 [bit-0]	PWR0K		R356 *1K/F_4 NC BBS_BIT0
GNT2# / GPIO53	ESI strap (Server only)	PWR0K	Should not be pull-down (weak pull-up 20K)	R381 *1K/F_4 NC BBS_BIT1 12
NV_ALE	Intel Anti-Theft HDD protection Only for Interposer	PWR0K	0 = Disable (Internal pull-down 20kohm)	
NV_CLE	DMI Termination voltage	PWR0K	weak pull-down 20kohm	+1.8V R343 2.2K_4 R344 1K/F_4 INV_CLE 13 H_SNB_IVB# 06
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+3V5 R164 1K/F_4 ACZ_SYNC
HDA_SDO	Flash Descriptor Security	PWR0K	0 = Override 1 = Default (weak pull-up 20K)	+3V5 R445 *1K/F_4 NC ACZ_SDOUT PT
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)	
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	
SPI_MOSI	ITPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable	

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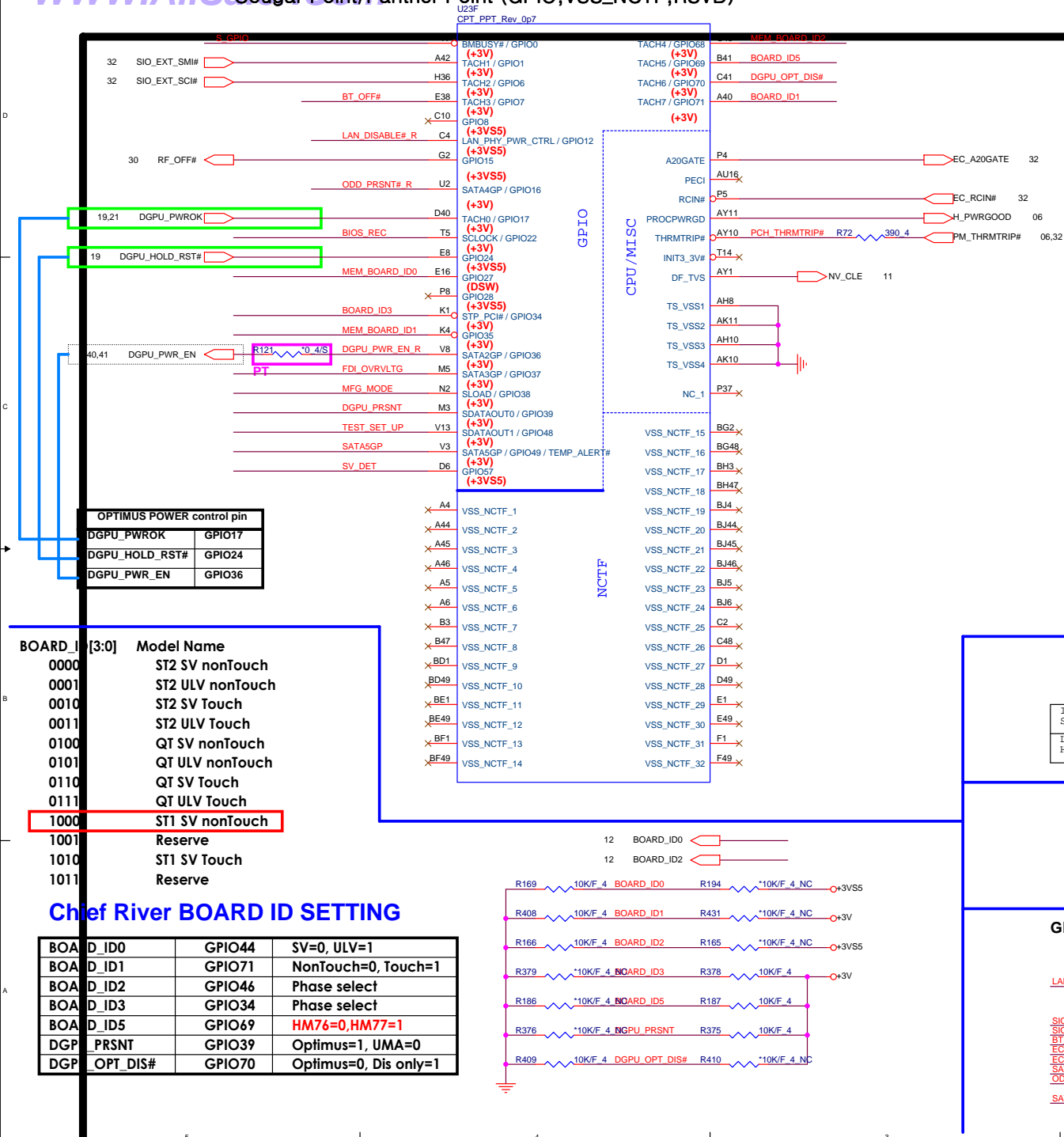
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Size Document Number

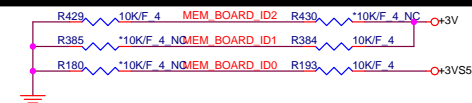
PCH 2/6 (HDA/RTC/SATA/SPI)

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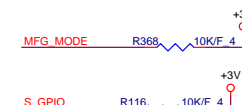
Default: HYNIX DDR3-1600 2GB



System Memory BOARD ID SETTING

	GPIO68 MEM_BOARD_ID2	GPIO35 MEM_BOARD_ID1	GPIO27 MEM_BOARD_ID0
HYNIX DDR3-1600 2GB	0	0	0
SAMSUNG DDR3-1600 2GB	0	0	1
On Board DDR3 N.C	0	1	1
RESERVE	0	1	0
RESERVE	1	0	0
RESERVE	1	0	1
RESERVE	1	1	1
RESERVE	1	1	0

MFG-TEST



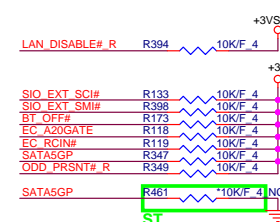
Intel ME Crypto Transport Layer Security (TLS) cipher suite
Low = Disable (Default)
High = Enable

BIOS RECOVERY High = Disable (Default)
Low = Enable

TEST SET_UP R102 10K/F 4 +3V
SV_SET_UP
High = Strong (Default)

R152 100K/F 4 SV_DET
TEST DETECT
Low = Default

GPIO Pull-up/Pull-down(CLG)

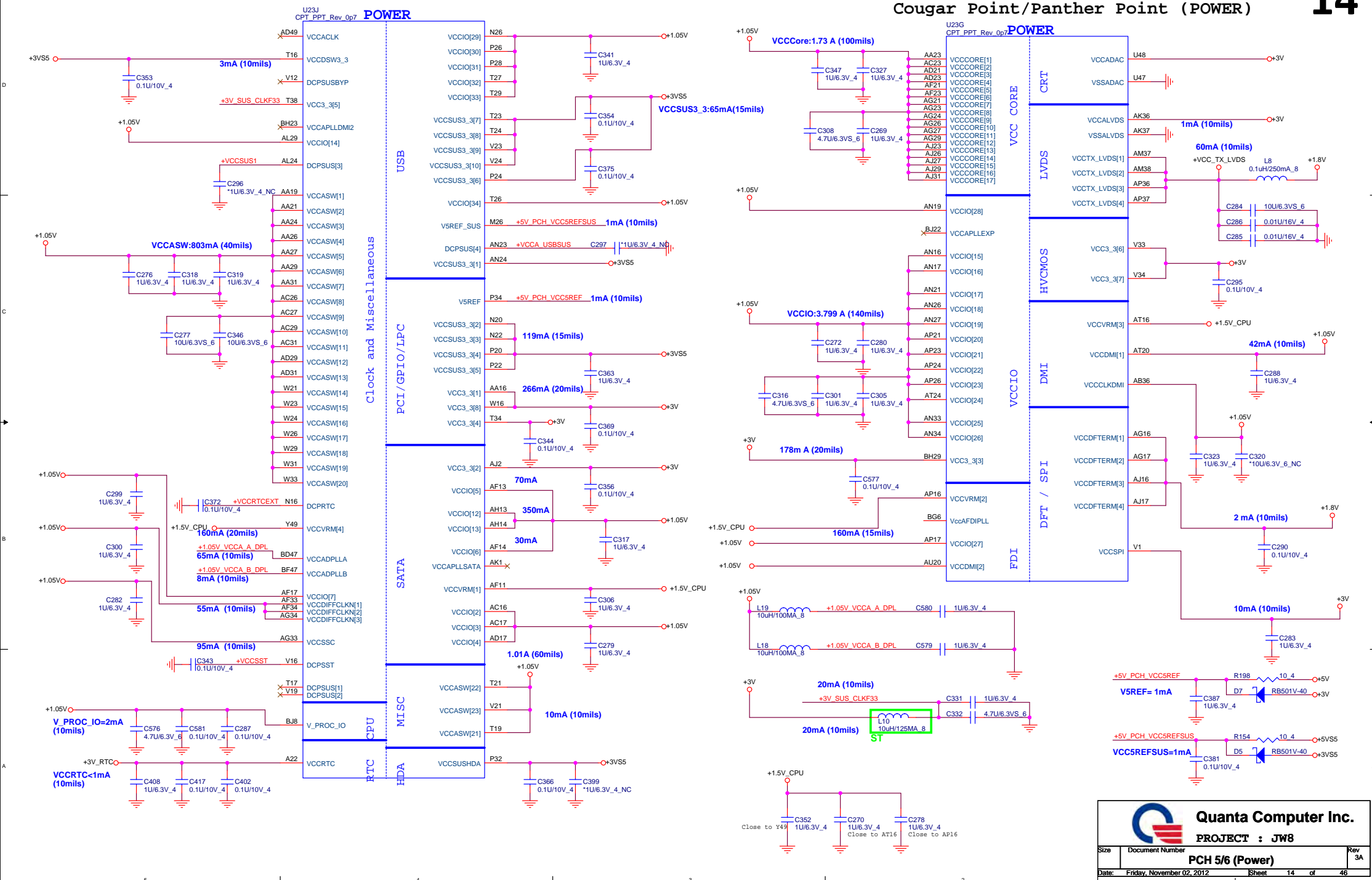


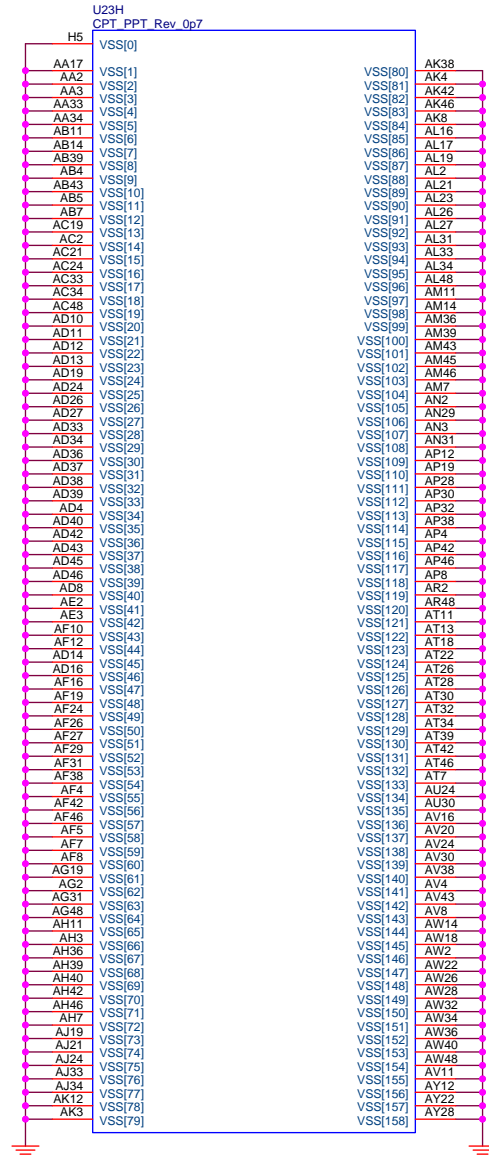
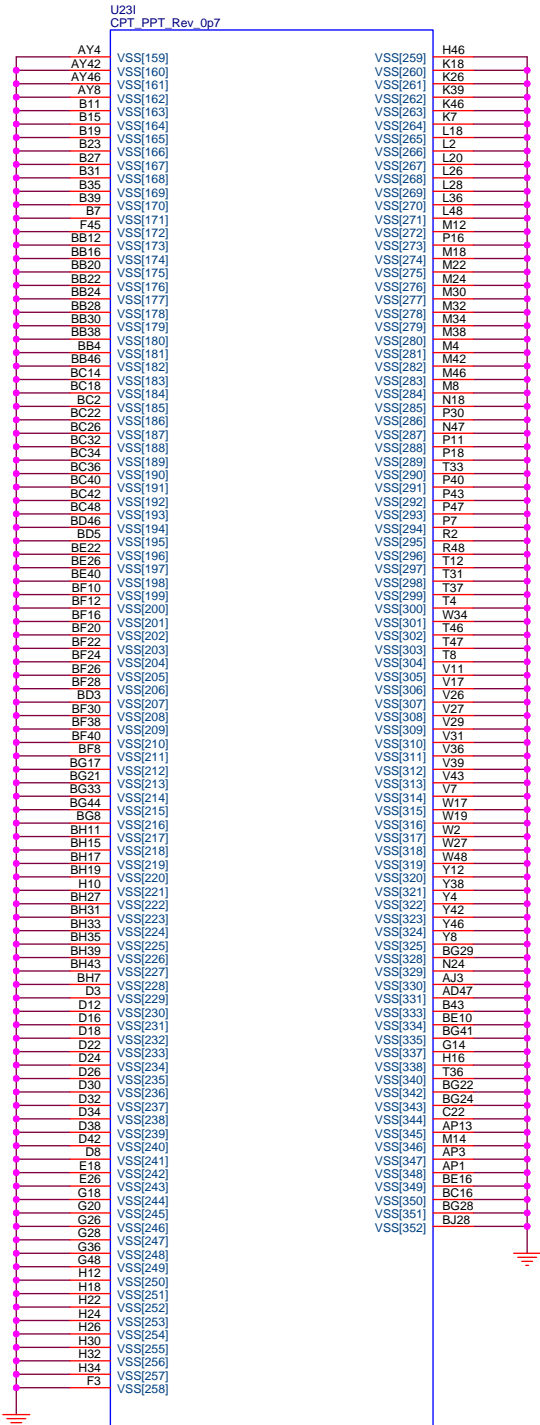
R138 100K/F 4 FDI_OVRVLTS
FDI TERMINATION VOLTAGE OVERRIDE Reserved only

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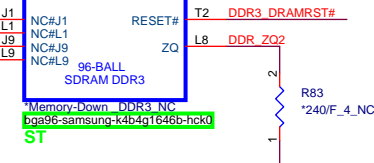
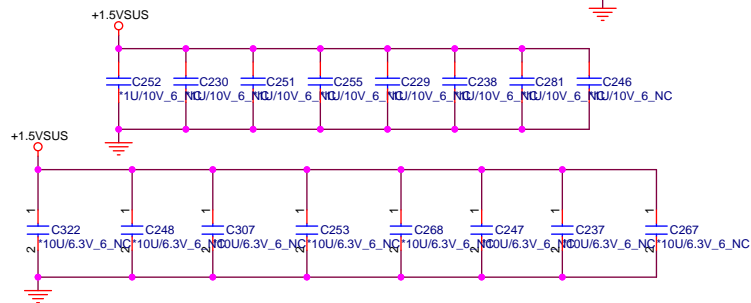
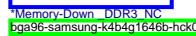
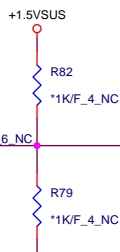
Size	Document Number	PCH 4/6 (GPIO)	Rev 3A
Date:	Friday, November 02, 2012	Sheet 13 of 46	

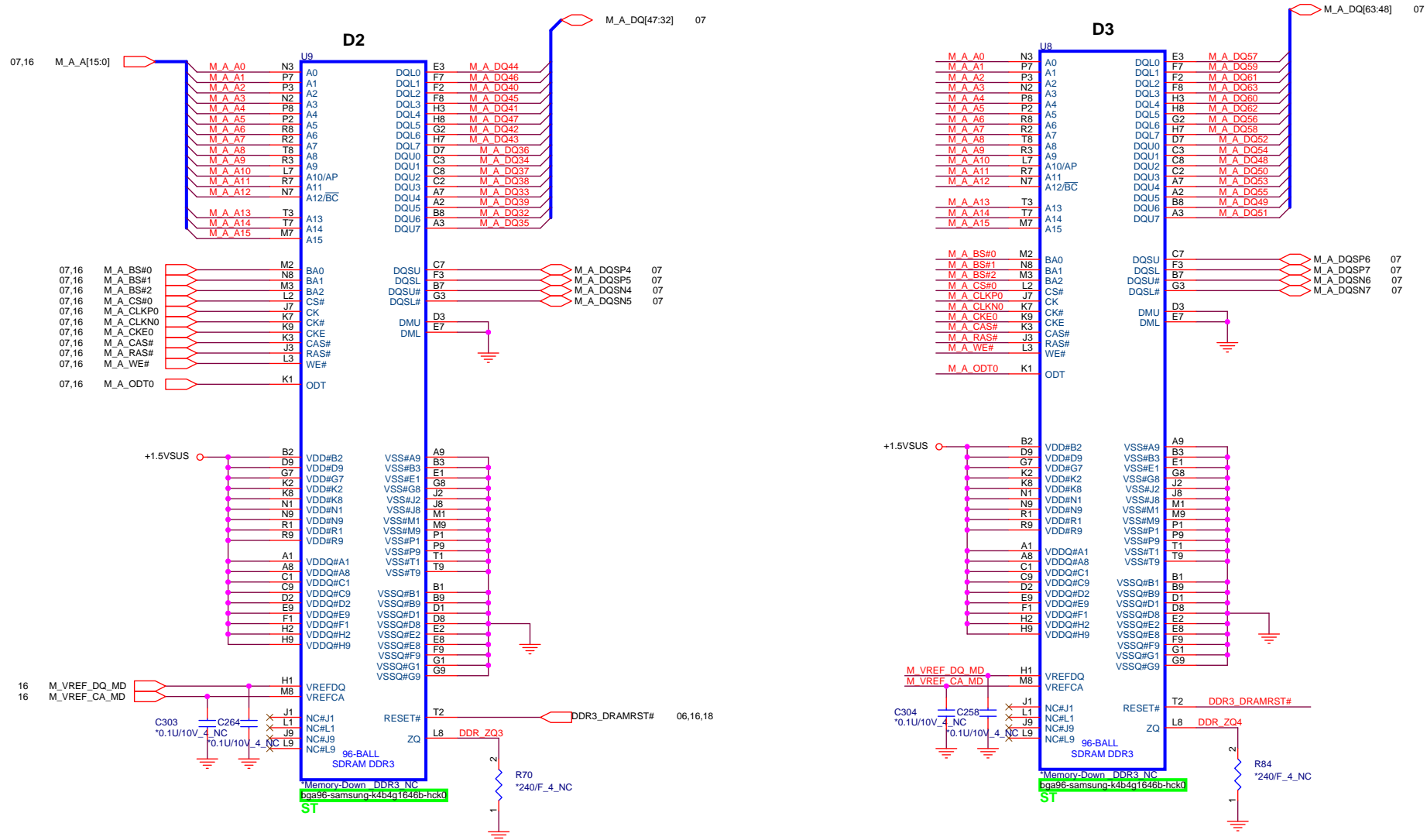
Cougar Point/Panther Point (POWER)





+0.75V_DDR_VTT

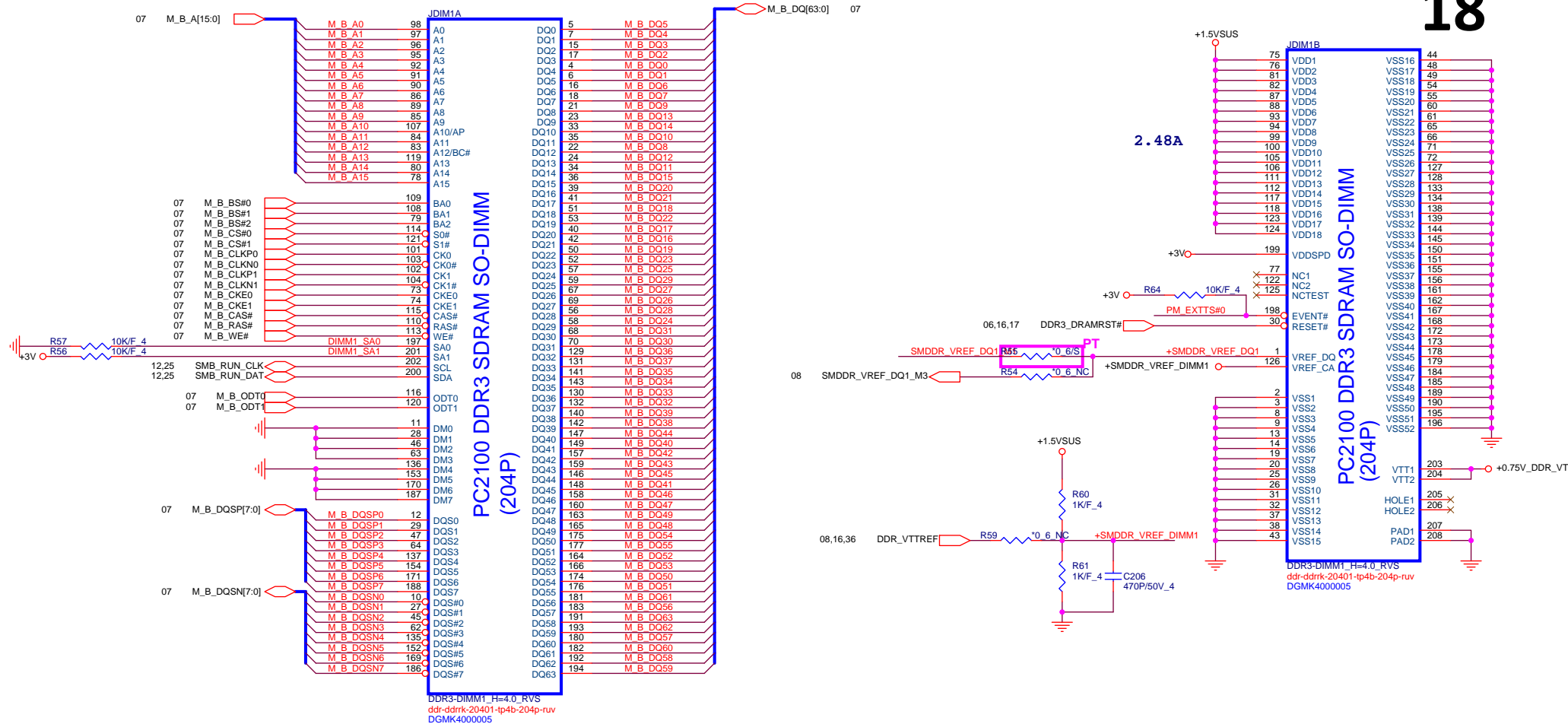




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Size	Document Number	Rev
	DDR3 (A) On Board_B,1Rank	3A
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FBA_ODT_L FBA_CMD2 R49 Dis@10K/F 4
FBA_ODT_H FBA_CMD18 R238 Dis@10K/F 4
FBA_RST# FBA_CMD5 R39 Dis@10K/F 4
FBA_CKE_L FBA_CMD3 R326 Dis@10K/F 4
FBA_CKE_H FBA_CMD19 R9 Dis@10K/F 4

TP24 FBA_CMD1 23 FBA_CMD0 C27 FBA_CMD0
23 FBA_CMD2 E24 FBA_CMD2
23 FBA_CMD3 F24 FBA_CMD3
23 FBA_CMD4 D27 FBA_CMD4
23 FBA_CMD5 D26 FBA_CMD5
23 FBA_CMD6 F25 FBA_CMD6
23 FBA_CMD7 F26 FBA_CMD7
23 FBA_CMD8 F23 FBA_CMD8
23 FBA_CMD9 G22 FBA_CMD9
23 FBA_CMD10 G23 FBA_CMD10
23 FBA_CMD11 G24 FBA_CMD11
23 FBA_CMD12 F27 FBA_CMD12
23 FBA_CMD13 G25 FBA_CMD13
23 FBA_CMD14 G27 FBA_CMD14
23 FBA_CMD15 G26 FBA_CMD15
23 FBA_CMD16 M24 FBA_CMD16
23 FBA_CMD17 M23 FBA_CMD17
23 FBA_CMD18 K24 FBA_CMD18
23 FBA_CMD19 K23 FBA_CMD19
23 FBA_CMD20 M27 FBA_CMD20
23 FBA_CMD21 M26 FBA_CMD21
23 FBA_CMD22 M25 FBA_CMD22
23 FBA_CMD23 K26 FBA_CMD23
23 FBA_CMD24 K22 FBA_CMD24
23 FBA_CMD25 J23 FBA_CMD25
23 FBA_CMD26 J25 FBA_CMD26
23 FBA_CMD27 J24 FBA_CMD27
23 FBA_CMD28 K27 FBA_CMD28
23 FBA_CMD29 K25 FBA_CMD29
23 FBA_CMD30 J27 FBA_CMD30
23 FBA_CMD31 J26 FBA_CMD31

+1.5V_GFX R31 Dis@60.4/F FBA_DEBUG F22 FBA_DEBUG0
R25 Dis@60.4/F FBA_DEBUG1 J22 FBA_DEBUG1

23 VMA_CLK0 D24 FBA_CLK0
23 VMA_CLK0 D25 FBA_CLK0
23 VMA_CLK1 N22 FBA_CLK1
23 VMA_CLK1# M22 FBA_CLK1

FB_PLLAVDD = 55mA

+1.05V_GFX L7 Dis@PBV160808T-300Y-NFB_PLLAVDD F16 FB_PLLAVDD
C171 Dis@10U/6.3V 5
C145 Dis@0.1U/10V 4
C146 Dis@0.1U/10V 4
C167 Dis@0.1U/10V 4
P22 FB_PLLAVDD
H22 FB_DLLAVDD GF119
FB_DLLAVDD GF117

FB_DLLAVDD = 15mA

FBA_DQM0 D19 VMA_DM0 VMA_DM[7:0] 23
FBA_DQM1 D14 VMA_DM1
FBA_DQM2 C17 VMA_DM2
FBA_DQM3 C22 VMA_DM3
FBA_DQM4 P24 VMA_DM4
FBA_DQM5 W24 VMA_DM5
FBA_DQM6 AA25 VMA_DM6
FBA_DQM7 U25 VMA_DM7

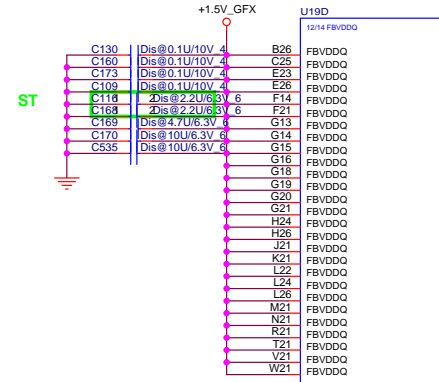
FBA_DQS_WP0 E19 VMA_WDQS0 VMA_WDQS[7:0] 23
FBA_DQS_WP1 C15 VMA_WDQS1
FBA_DQS_WP2 B16 VMA_WDQS2
FBA_DQS_WP3 B22 VMA_WDQS3
FBA_DQS_WP4 R25 VMA_WDQS4
FBA_DQS_WP5 W23 VMA_WDQS5
FBA_DQS_WP6 AB26 VMA_WDQS6
FBA_DQS_WP7 T26 VMA_WDQS7

FBA_DQS_RN0 F19 VMA_RDQS0 VMA_RDQS[7:0] 23
FBA_DQS_RN1 C14 VMA_RDQS1
FBA_DQS_RN2 A16 VMA_RDQS2
FBA_DQS_RN3 A22 VMA_RDQS3
FBA_DQS_RN4 P25 VMA_RDQS4
FBA_DQS_RN5 W22 VMA_RDQS5
FBA_DQS_RN6 AB27 VMA_RDQS6
FBA_DQS_RN7 T27 VMA_RDQS7

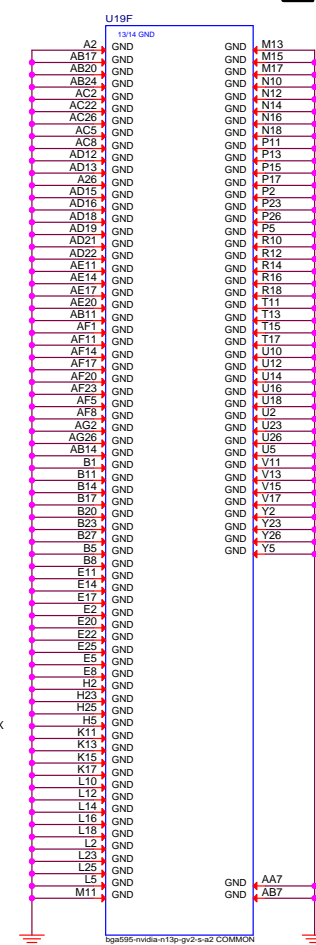
FB_VREF_PROBE D23 FB_VREF_PROBE TP6

VMA_DQ[63:0] VMA_DQ[63:0] 23

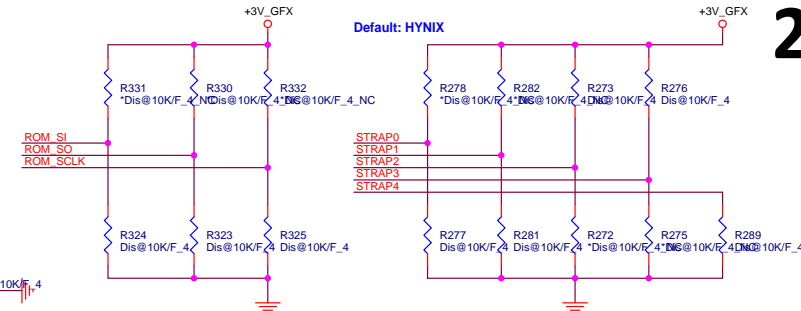
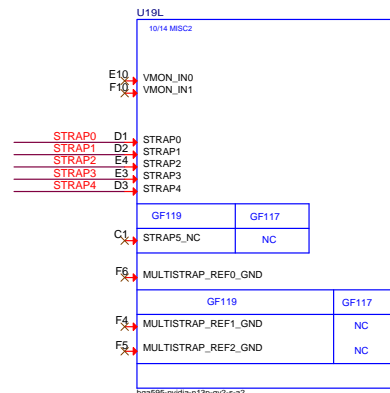
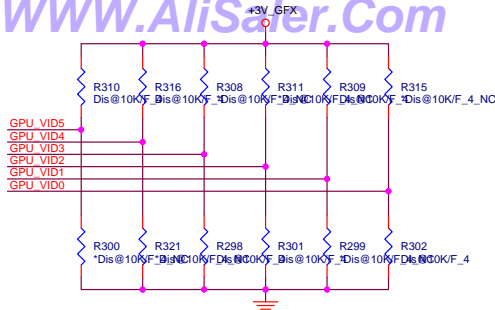
FBVDDQ + FBVDD = 3.116A



FB_CAL_PD_VDDQ D22 FB_CAL_PD_VDDQ R283 Dis@40.2/F 4 +1.5V_GFX
FB_CAL_PU_GND C24 FB_CAL_PU_GND R279 Dis@42.2/F 4
FB_CAL_TERM_GND B25 FB_CAL_TERM_GND R274 Dis@51.1/F 4







Binary Strap Mode Mapping

Strap Pin name	Strap Mapping	Resistance	Polarity
ROM_SCLK	SMB_ALT_ADDR	10Kohm	Pull-down to GND
ROM_SI	SUB_VENDOR	10Kohm	Pull-UP to 3V3 if VBIOS ROM Exists Pull-down to GND (no dispaly)
ROM_SO	VGA_DEVICE	10Kohm	Pull-down to GND (no dispaly)
STRAP0	RAMCFG[0]	10Kohm	USER defined
STRAP1	RAMCFG[1]	10Kohm	USER defined
STRAP2	RAMCFG[2]	10Kohm	USER defined
STRAP3	RAMCFG[3]	10Kohm	USER defined
STRAP4	PCIE_MAX_SPEED	10Kohm	Pull-down to GND

VRAM Configuration Table

RAMCFG [3:0]	DESCRIPTION	Vendor	Vendor P/N	QCI P/N	
0000		Reserved			
1100	DDR3 128Mx16x4, 64bit, 2Gb,900MHz	HYNIX	H5TQ2G63DPR-11C	AKD5MGWTW16	
1011	DDR3 128Mx16x4, 64bit, 2Gb,900MHz	SAMSUNG	K4W2G1646E-BC11	AKD5MGWT526	
	DDR3 256Mx16x4, 64bit, 4Gb,900MHz	HYNIX	H5TQ4G63MFR-11C	AKD5PGWTW04	
	DDR3 256Mx16x4, 64bit, 4Gb,900MHz	SAMSUNG	K4W4G1646B-HC11	AKD5MGWT516	

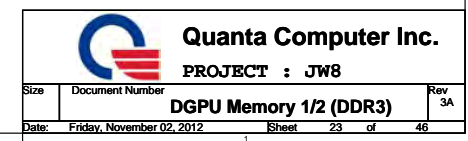
GPIO ASSIGNMENTS

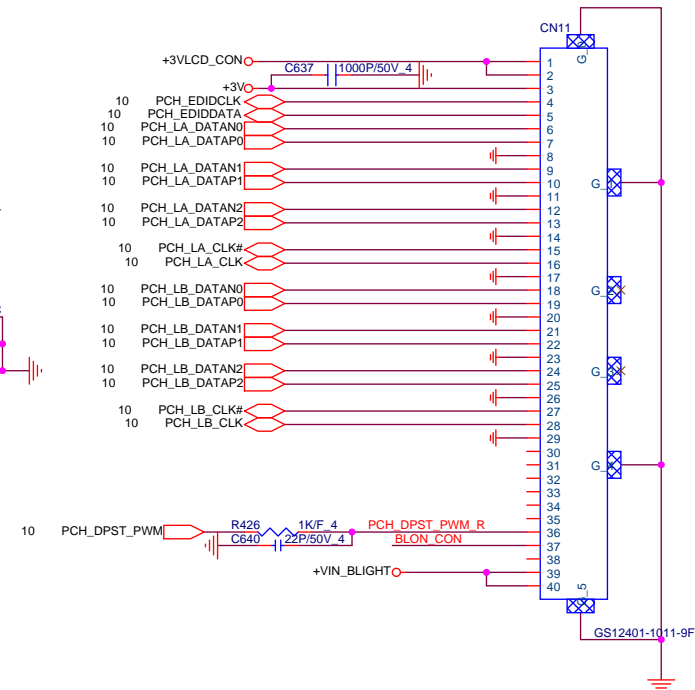
GPIO	I/O	PIN	USAGE
0	OUT	GPU_VID4	GPU CORE_VDD VID4
1	OUT	GPU_VID3	GPU CORE_VDD VID3
2	OUT	LCD_BL_PWM	LCD BACKLIGHT PWM
3	OUT	LCD_VCC	PANEL POWER ENABLE
4	OUT	LCD_BLEN	PANEL BACKLIGHT ENABLE
5	OUT	GPU_VID1	GPU CORE_VDD VID1
6	OUT	GPU_VID2	GPU CORE_VDD VID2
7	OUT	3D VISION	3D VISION LEFT/RIGHT VISION
8	I/O	OVERT	ACTIVE LOW THERMAL OVER TEMP
9	I/O	ALERT	ACTIVE LOW THERMAL ALERT
10	OUT	MEM VREF	MEMORY VREF CONTROL
11	OUT	GPU_VID0	GPU CORE_VDD VID0
12	IN	PWR_LEVEL	Power Detect ,HIGH=AC, LOW=DC
13	OUT	GPU_VID5	GPU CORE_VDD VID5
14	IN	HPD_AB	HOT PLUG DETECT FOR IFPAB
15	IN	HPD_C	HOT PLUG DETECT FOR IFPC
16	OUT	MEM_VDD	MEMMORY VDD CONTROL
17	IN	HPD_D	HOT PLUG DETECT FOR IFPD
18	IN	HPD_E	HOT PLUG DETECT FOR IFPE
19	IN	HPD_F	HOT PLUG DETECT FOR IFPF
20/21		RESERVE	

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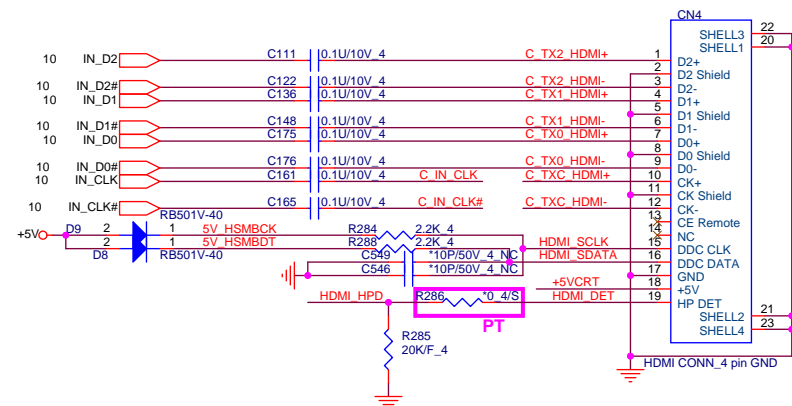
Date: Friday, November 02, 2012 Sheet 22 of 46

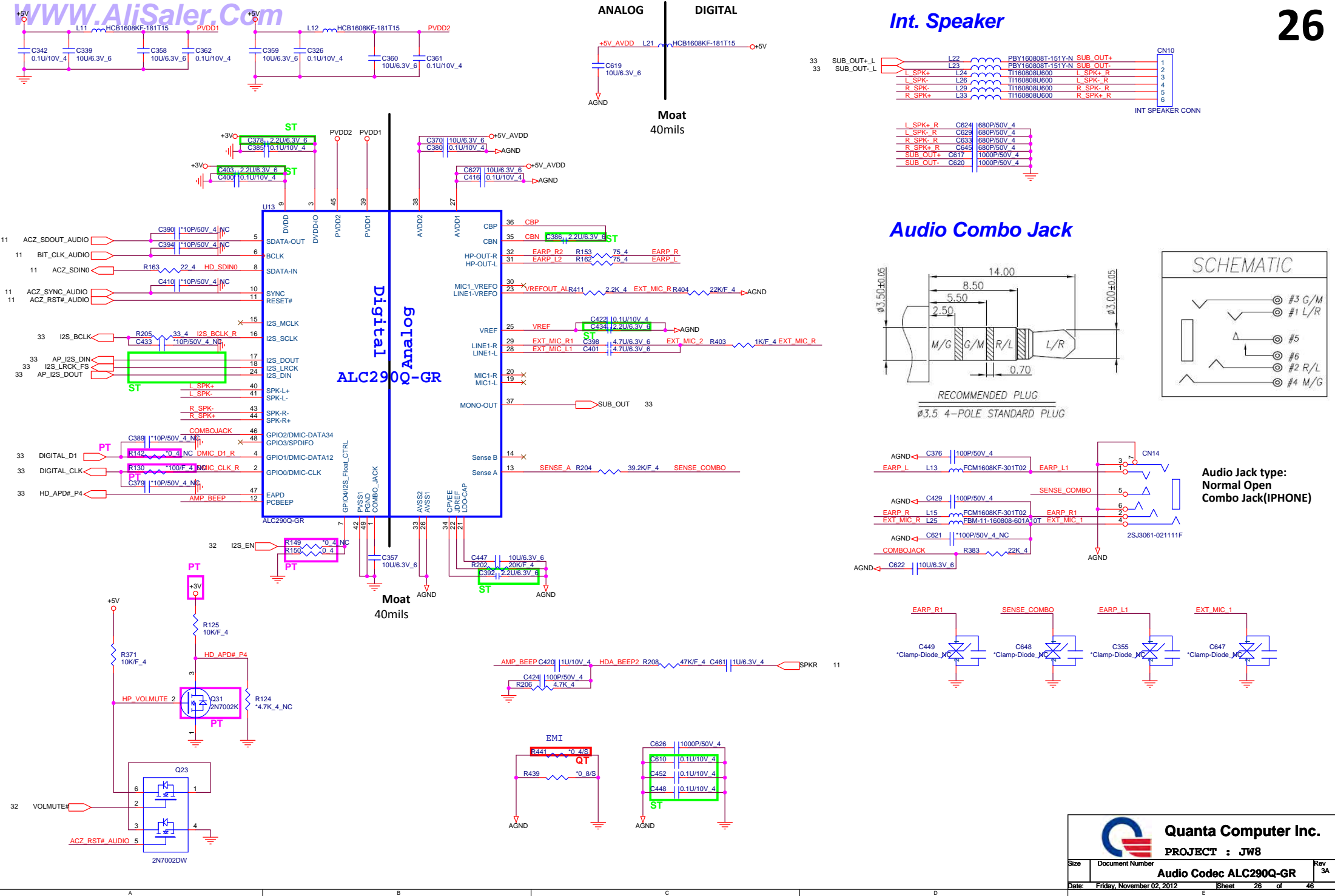
Size Document Number DGPU 4/5 (MIO/GPIO) Rev 3A

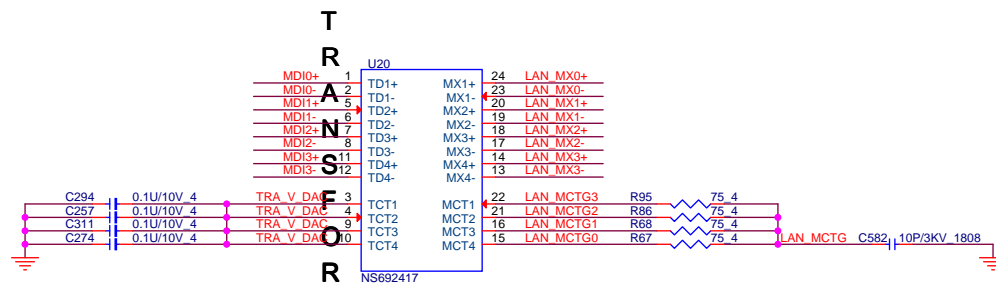
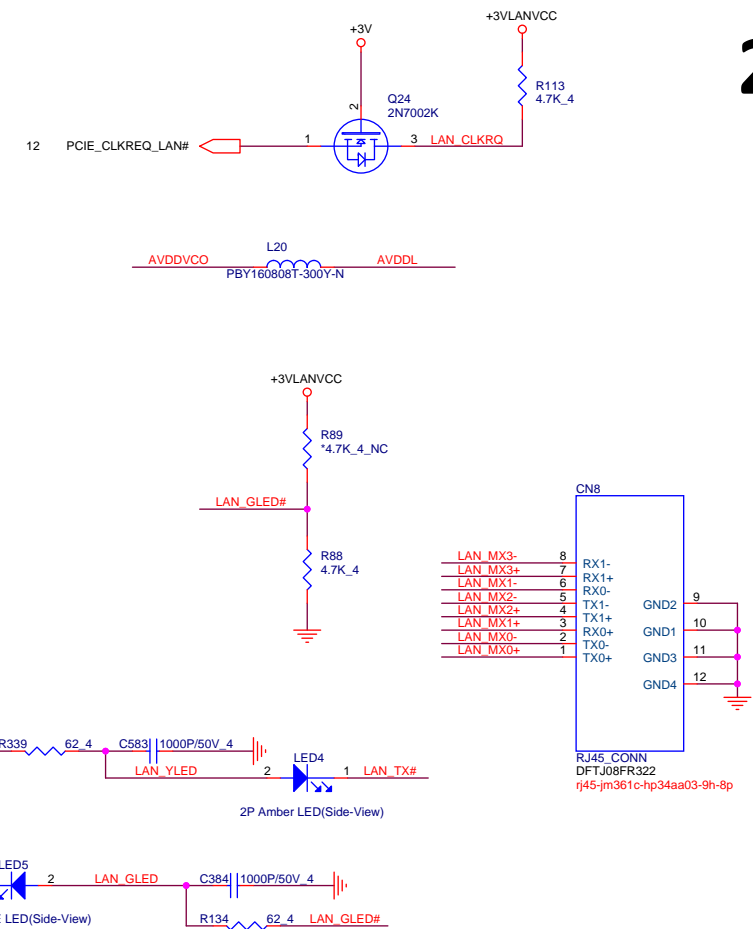
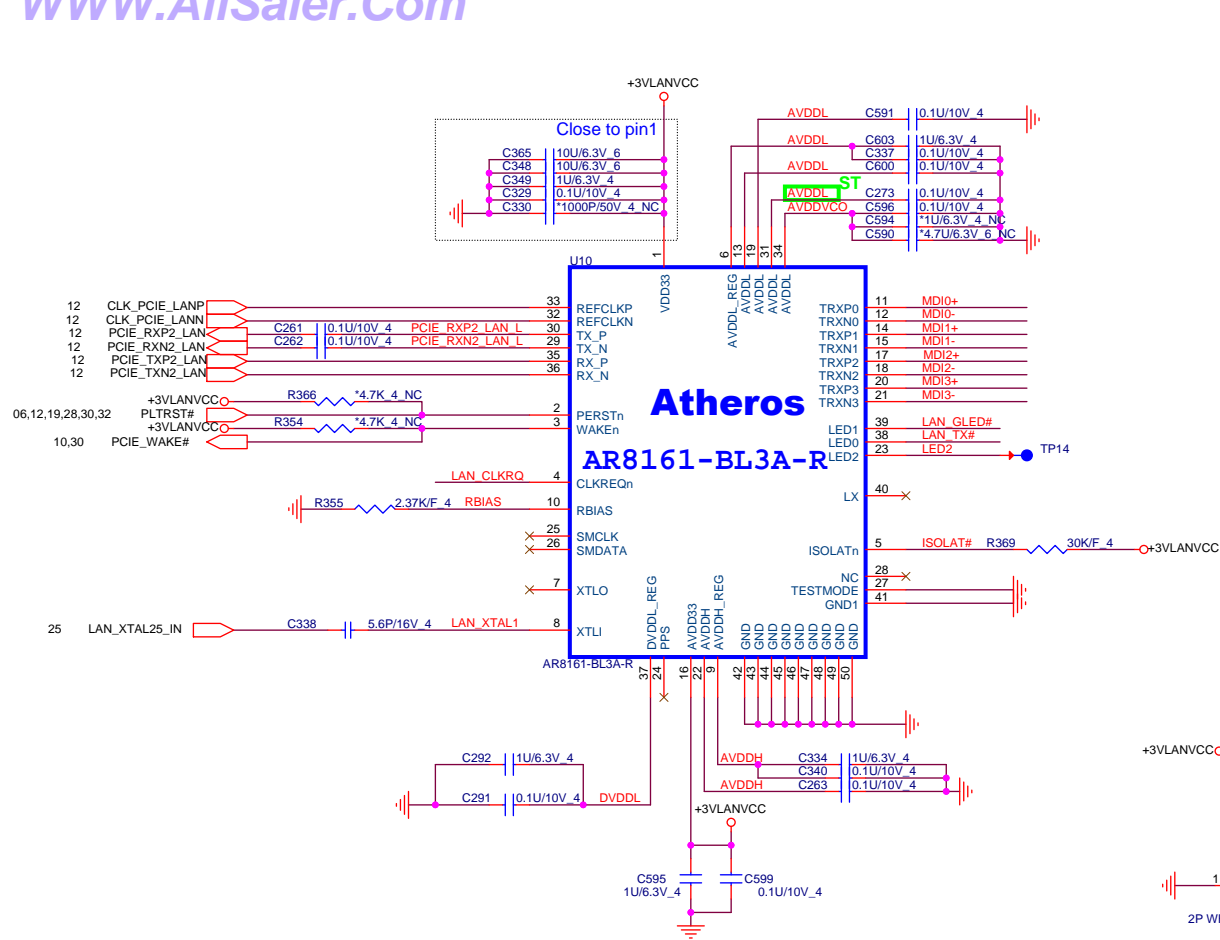




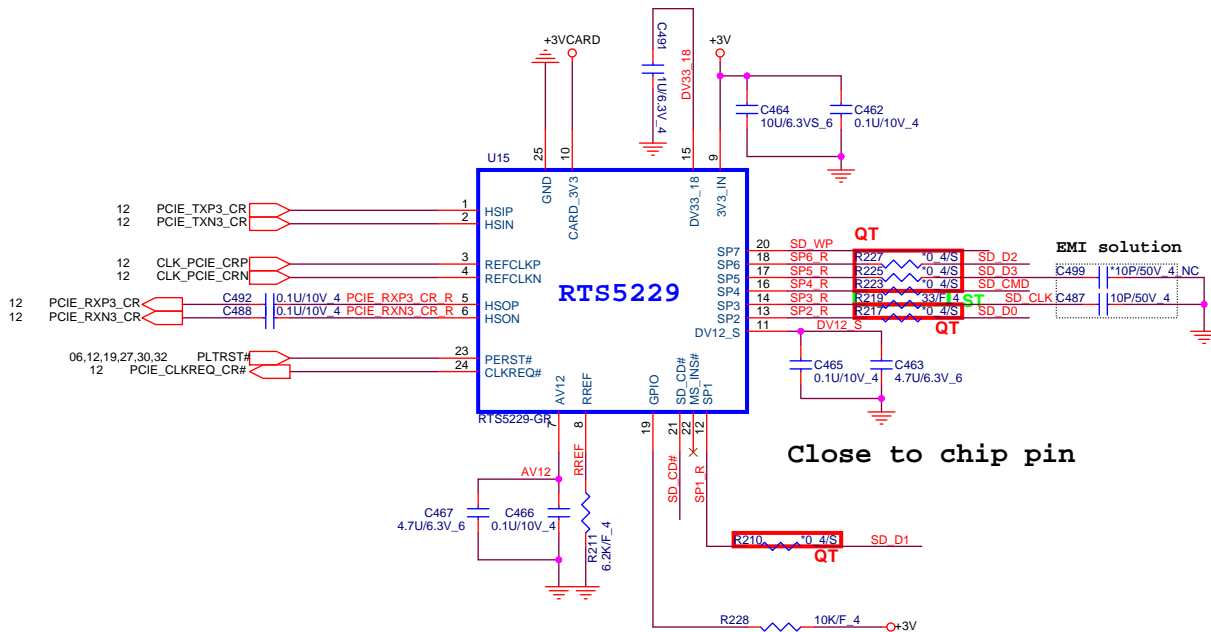
HDMI PORT



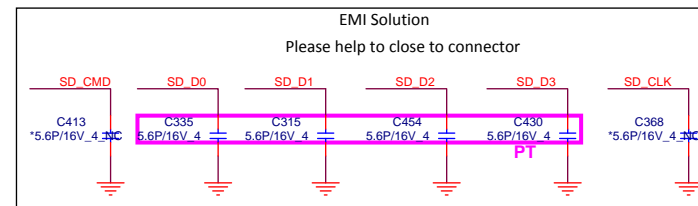




FCE: NS692417, DB0KL3LAN02
BOT: NA0069R LF, DB0KL3LAN01

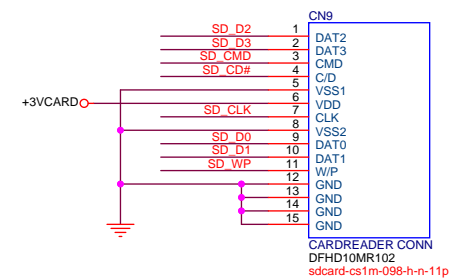
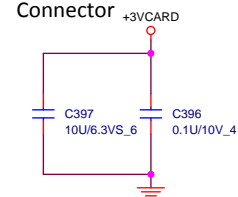


Share Pin

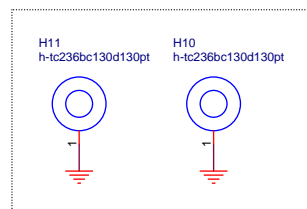


SD / MMC CARD READER

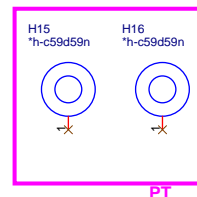
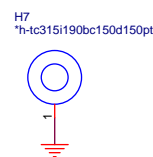
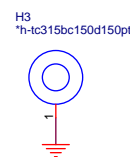
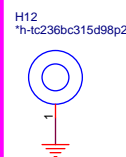
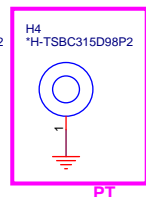
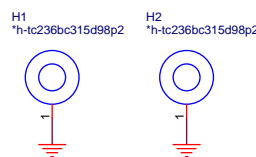
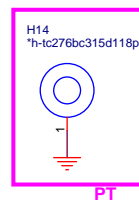
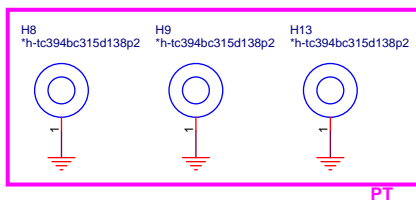
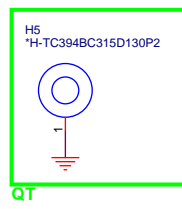
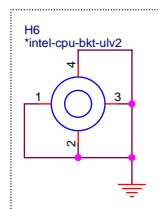
Place close to
Connector



Mini-PCIE

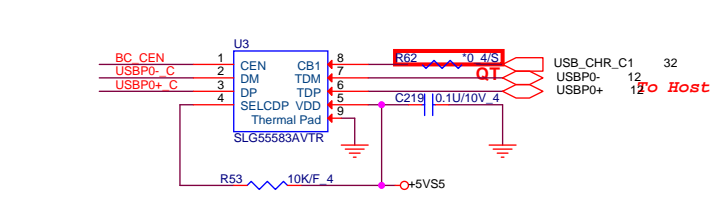


CPU BKT



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PROJECT : JW8

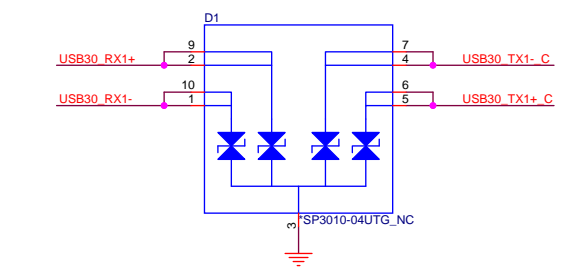
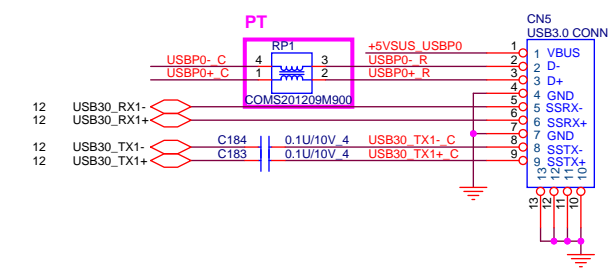
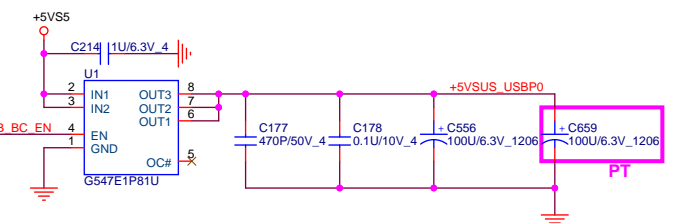
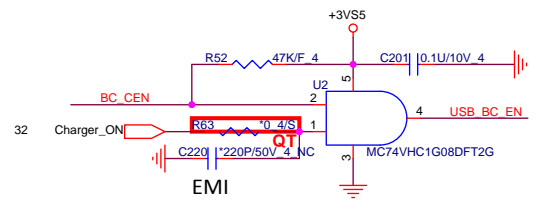
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	CR RTS5229-GR/Holes	3A
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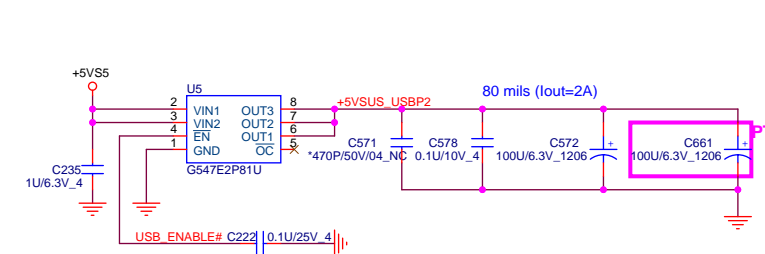
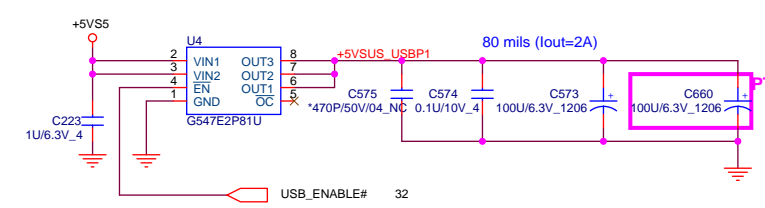
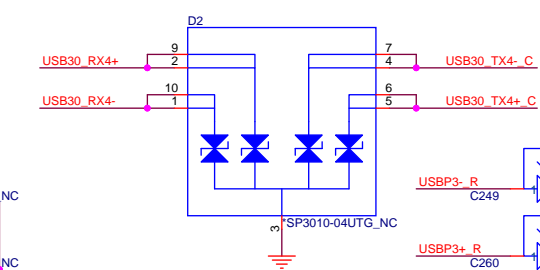
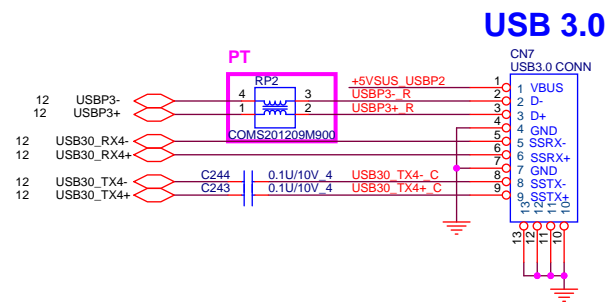
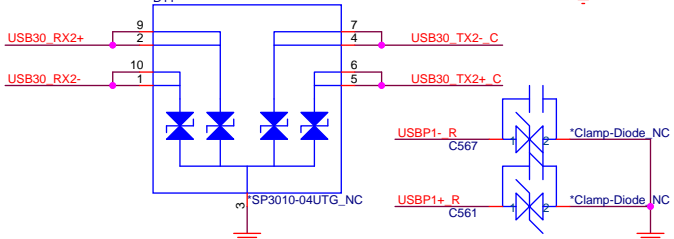
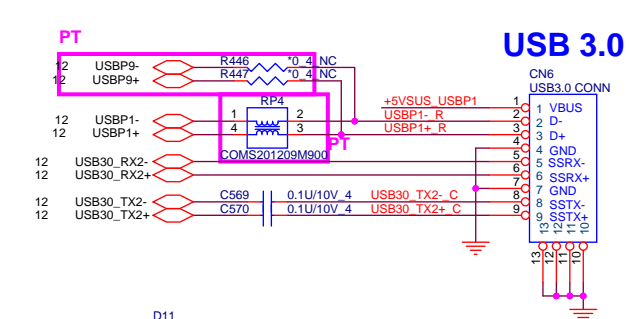
CB	SELCDP	Function
0	X	DCP autodetect with mouse/keyboard wakeup
1	0	80 charging with SDP only
1	1	80 charging with CDP or SDP only (depending on external device)

• USB Charge at S0 / S3 / S4 / S5 (Set by BIOS)

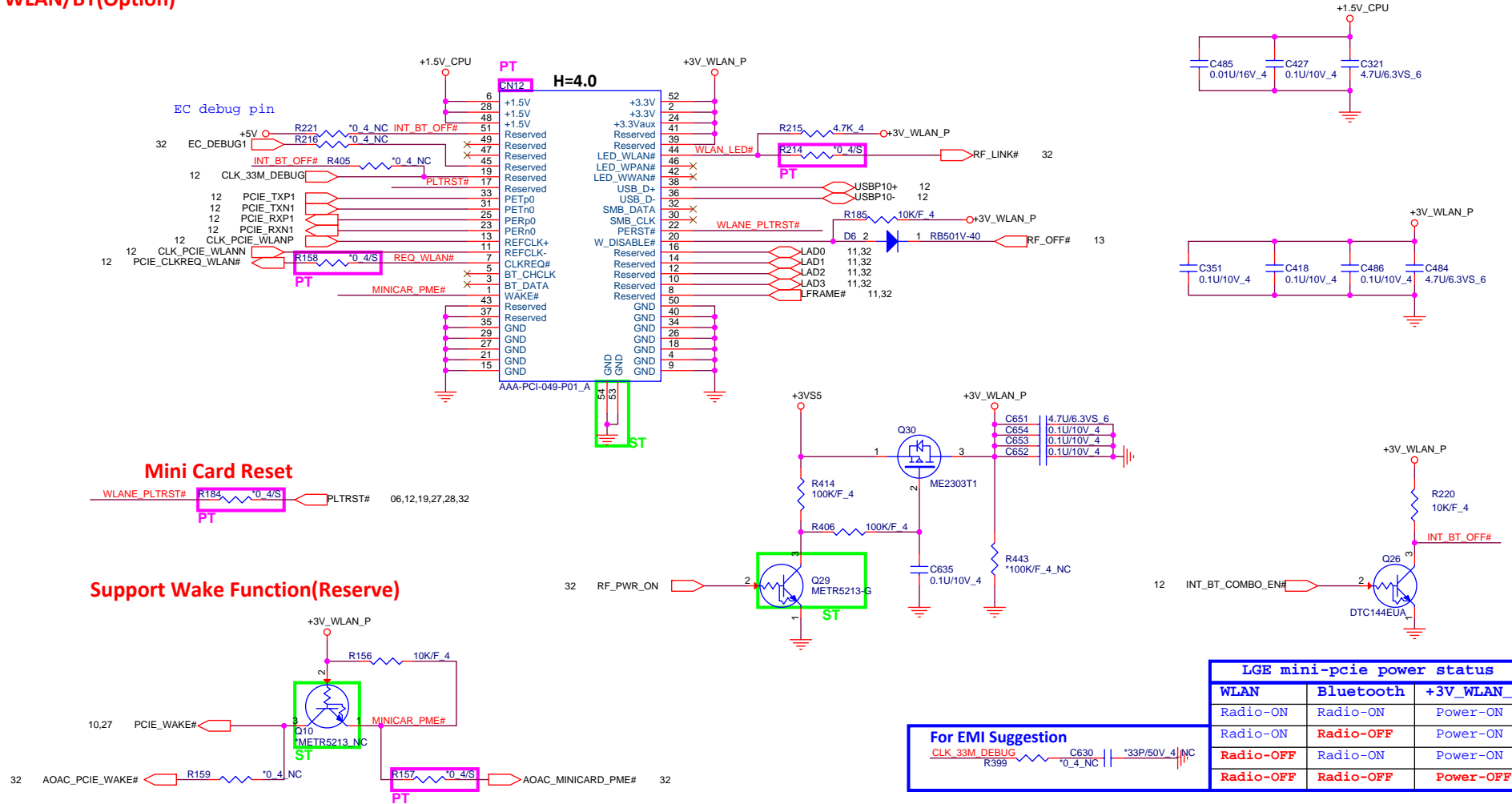
Current Battery Capacity	USB Charge (Set by BIOS)	S0		S3		S4/S5		EC wake up to read battery capacity from deep sleep mode	
		AC	DC	AC	DC	AC	DC		
> battery level (20%)	Enable	CDP	CDP	DCP	DCP	DCP	DCP	No	Yes
	Disable (Default)	CDP	CDP	Off	Off	Off	Off	No	No
<= battery level (20%)	Enable	CDP	CDP	DCP	Off	DCP	Off	No	No
	Disable (Default)	CDP	CDP	Off	Off	Off	Off	No	No



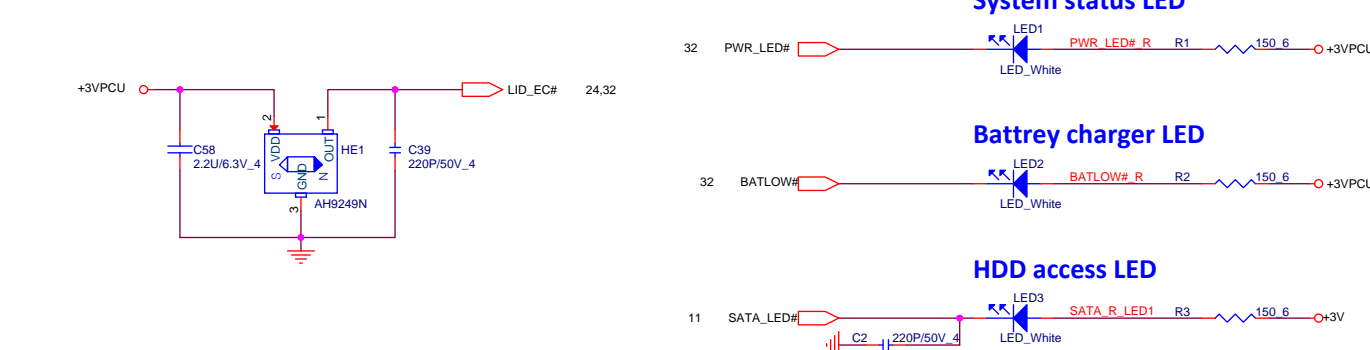
USB3.0/2.0 COMBO X 2

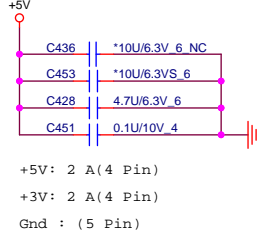
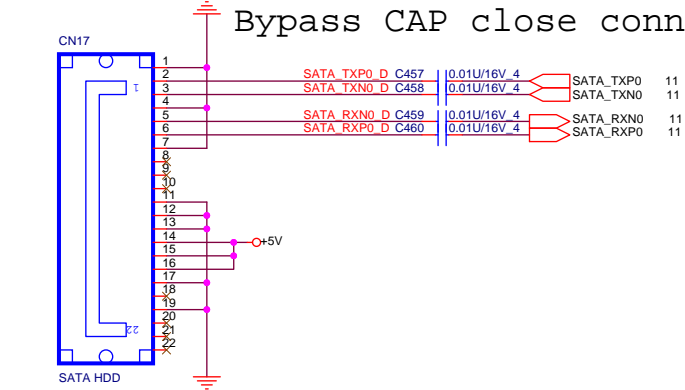


14,31,35,36,37,38,40,42,44 +5VS5

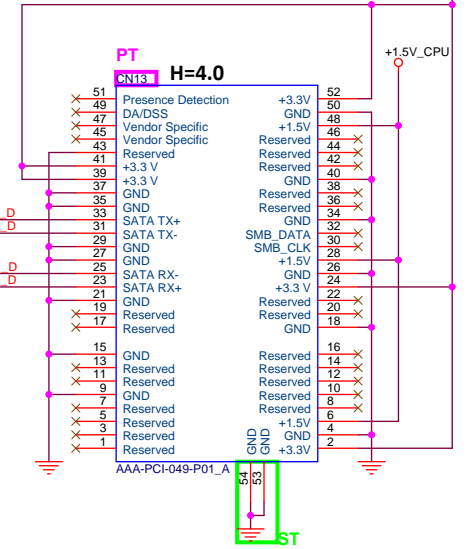
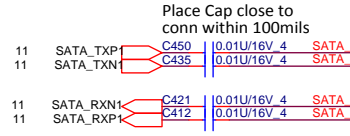


LED Status

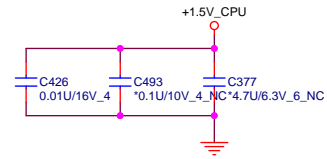
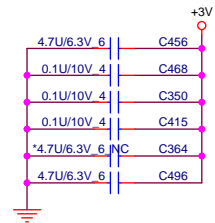
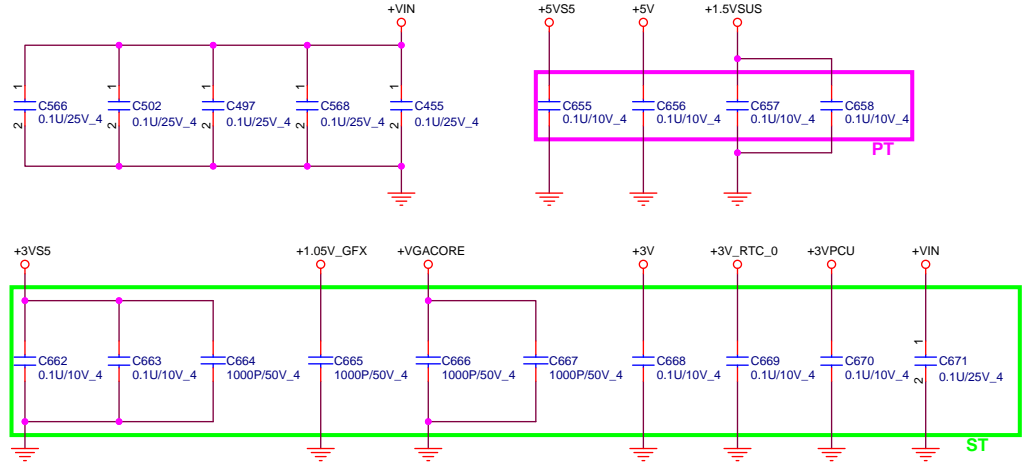




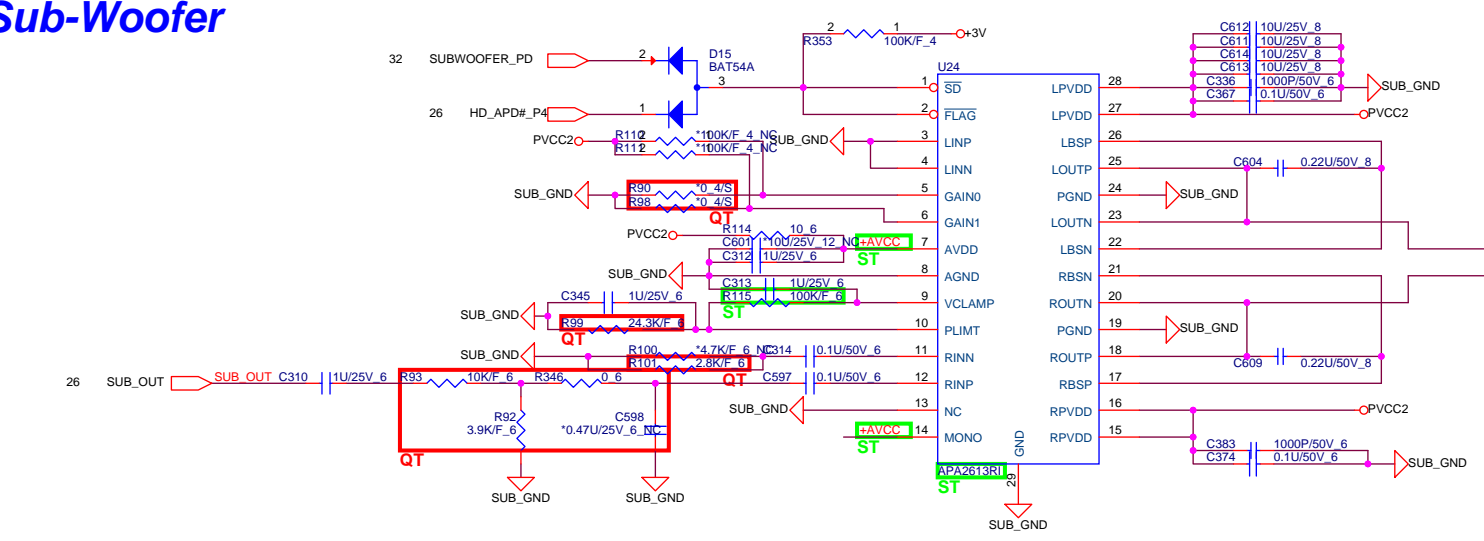
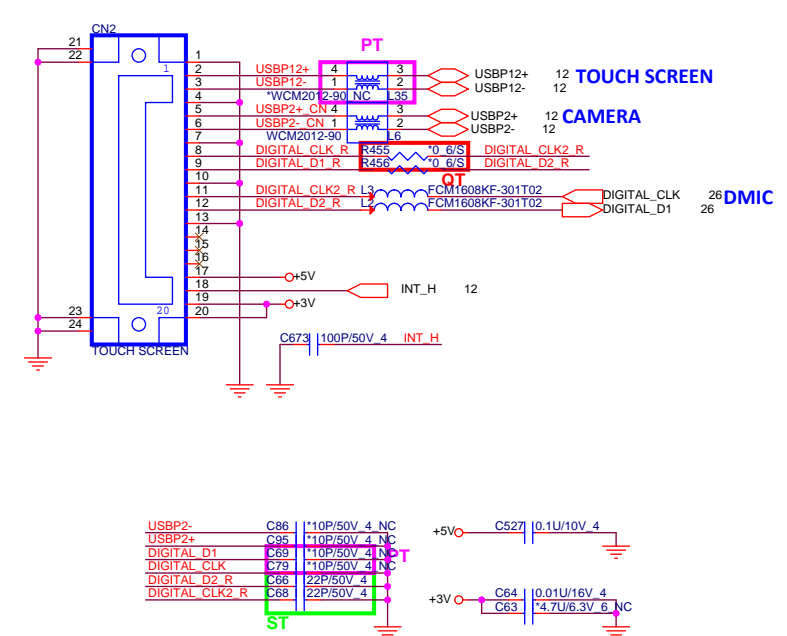
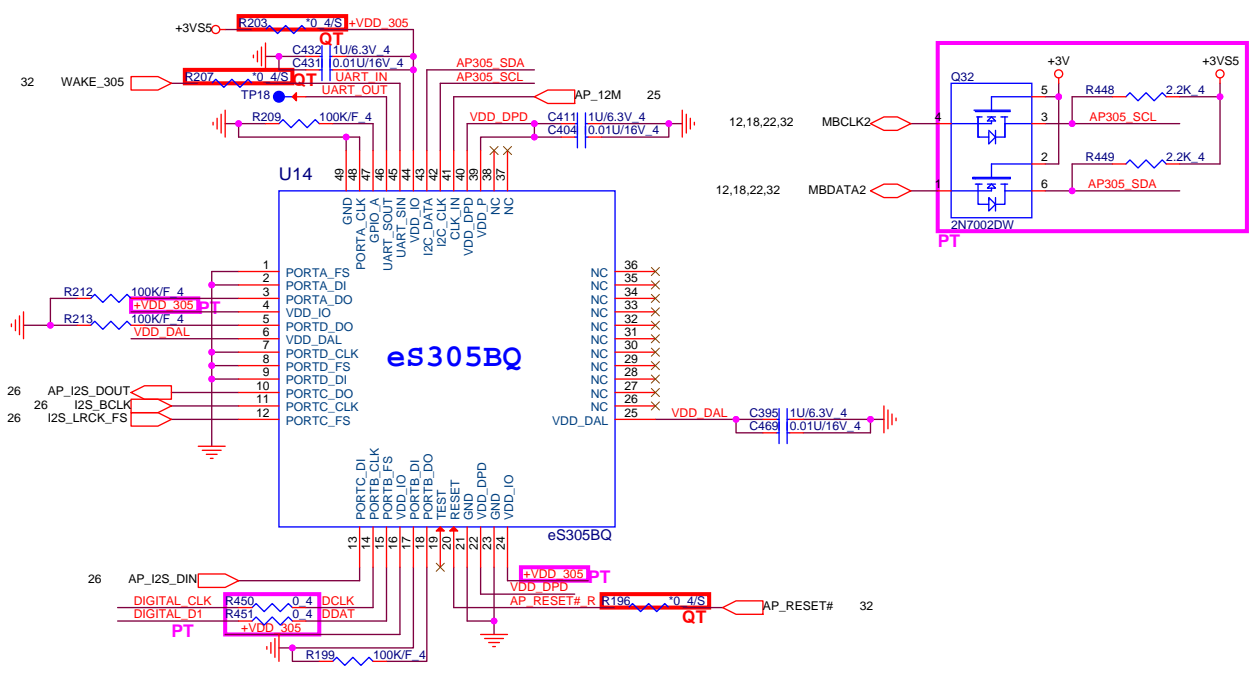
mSATA



EMI







PT

R112 100K 4

R91 100K 4

+VIN

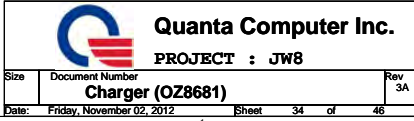
PVCC2

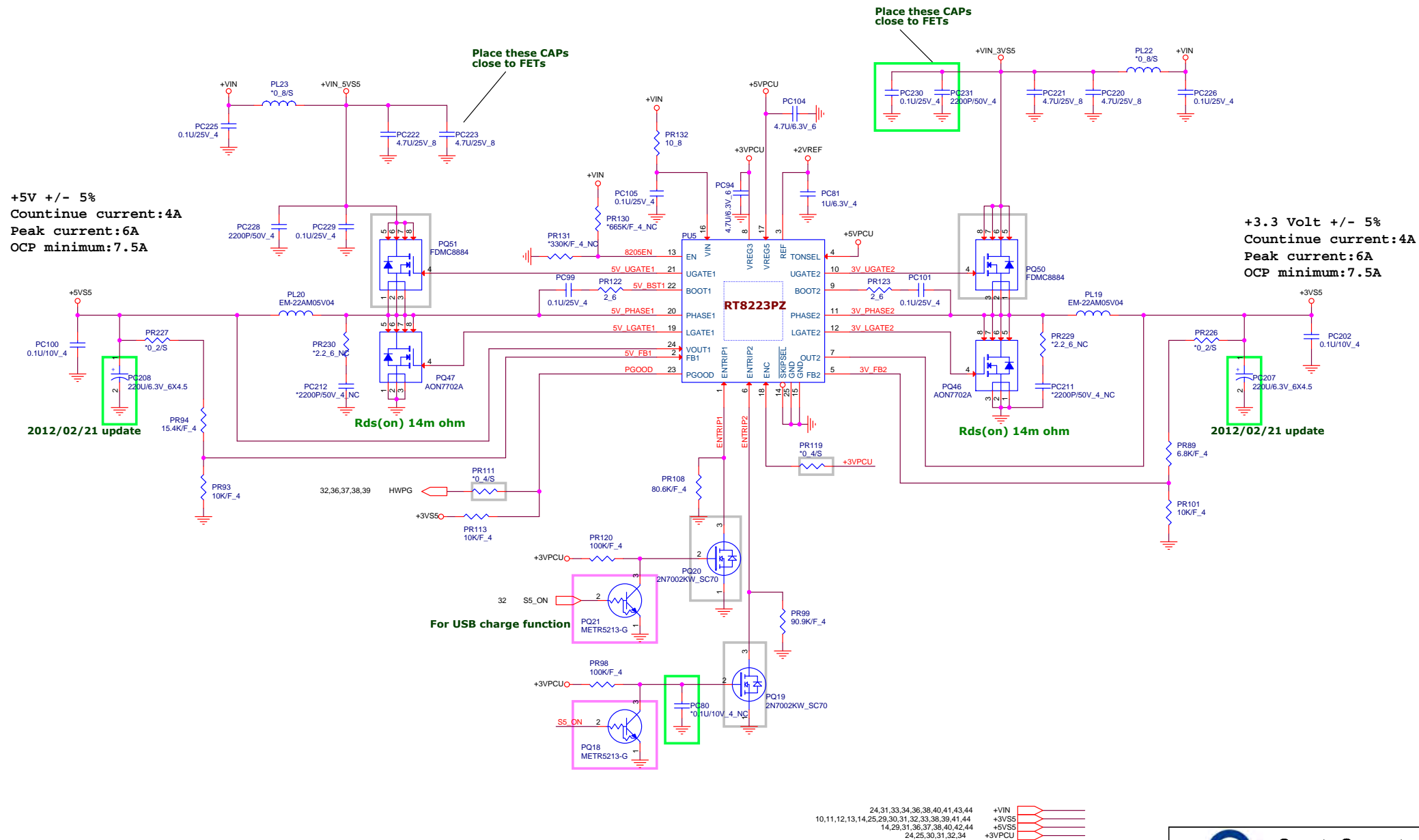
R120 100K 4

short0805

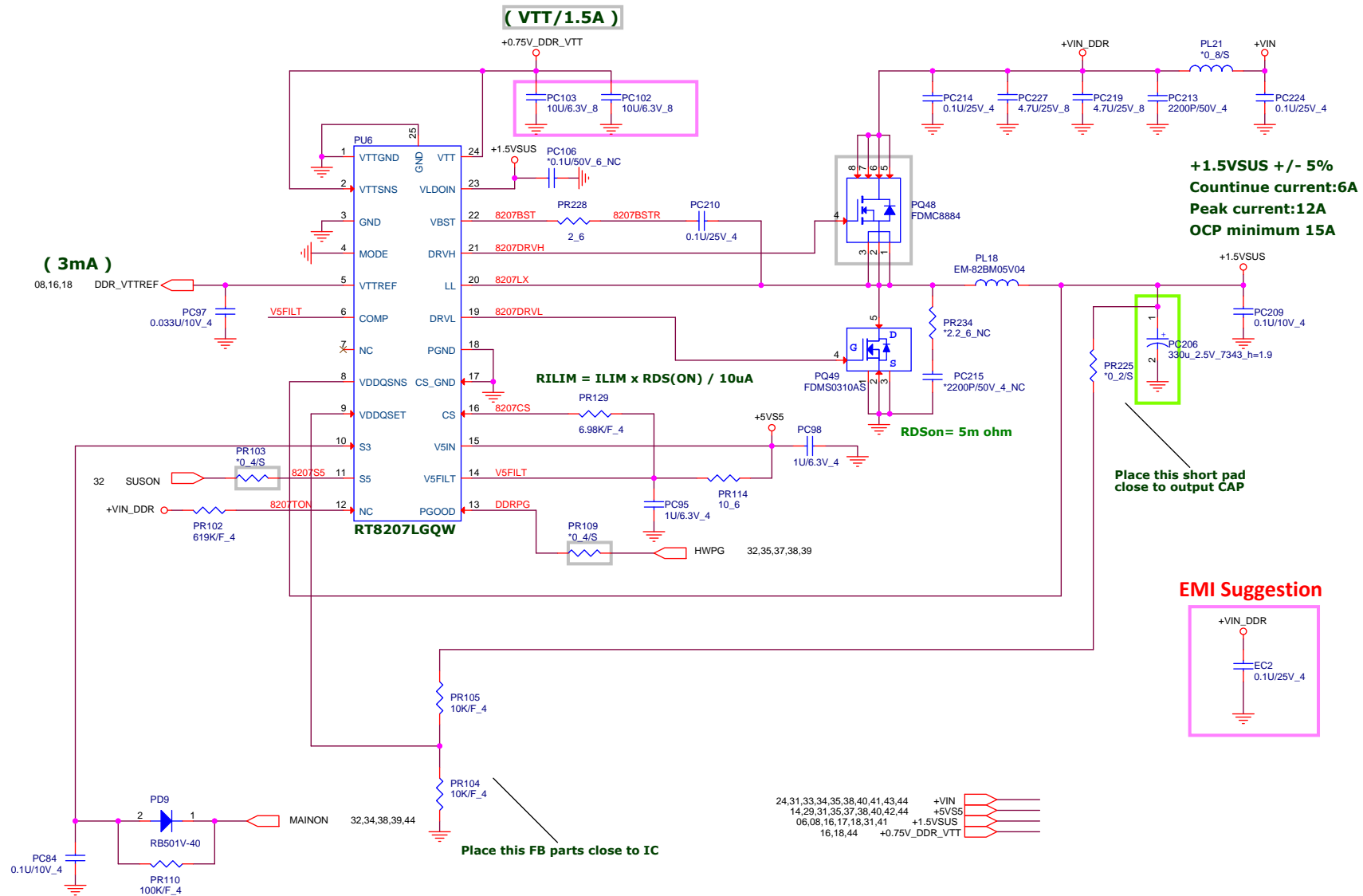
GAIN1	GAIN0	dB
0	0	20
0	1	26
1	0	32
1	1	36

ANC: APA2613RI-TRG, AL002613K00
TIC: TPA3111D1PWPR, AL003111K00



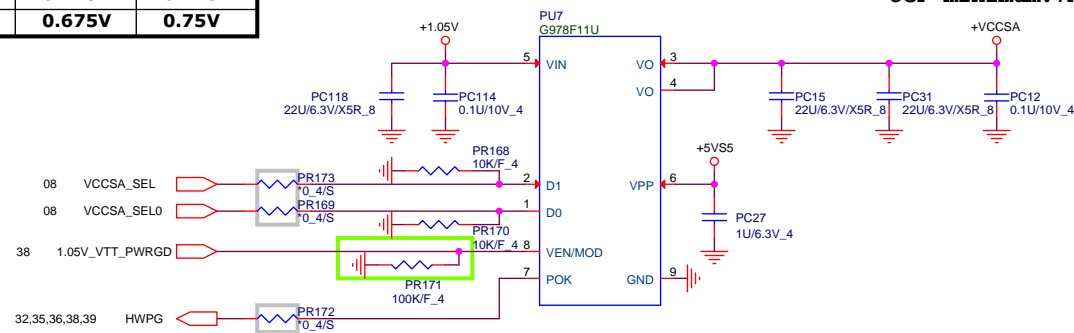


24,31,33,34,36,38,40,41,43,44 +VIN
10,11,12,13,14,25,29,30,31,32,33,38,39,41,44 +3VS5
14,29,31,36,37,38,40,42,44 +5VS5
24,25,30,31,32,34 +3VPCU



D0	D1	SV +VCCSA	ULV +VCCSA
0	0	0.9V	0.9V
0	1	0.8V	0.85V
1	0	0.725V	0.775V
1	1	0.675V	0.75V

+VCCSA Volt +/- 5%
 Countinue current:4A
 Peak current:6A
 OCP minimum:7A

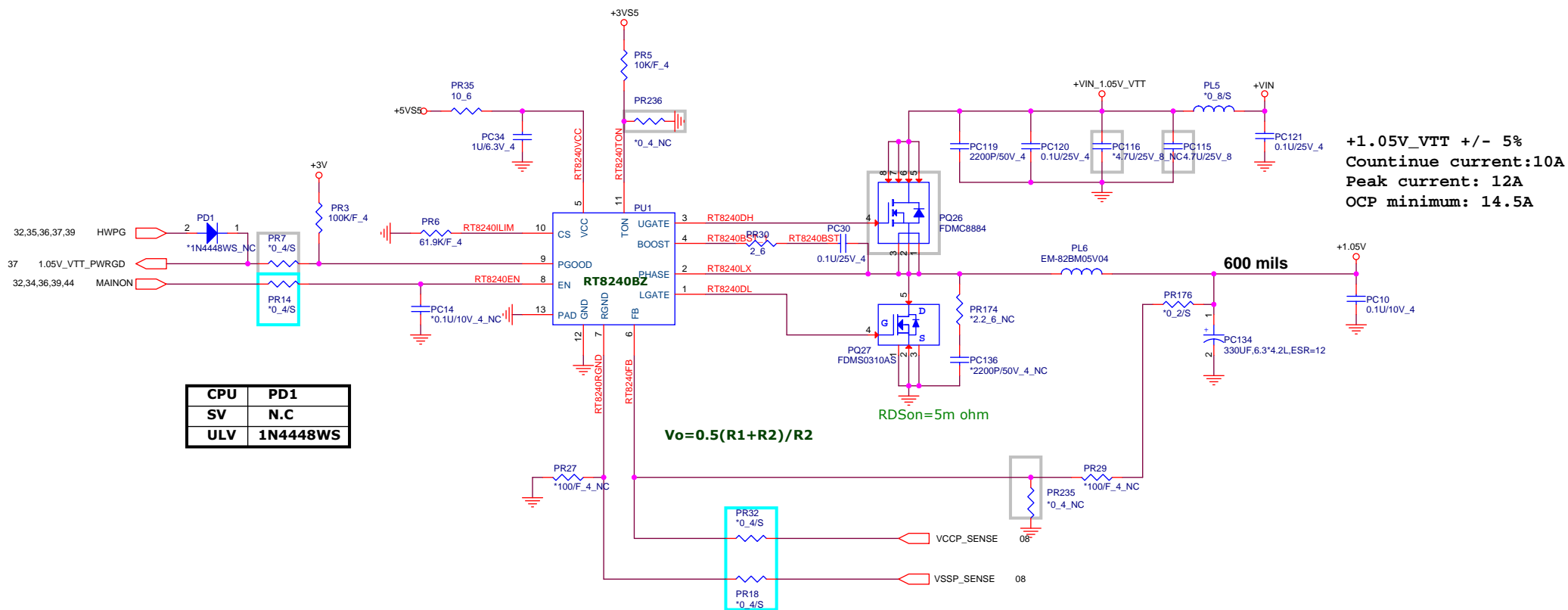


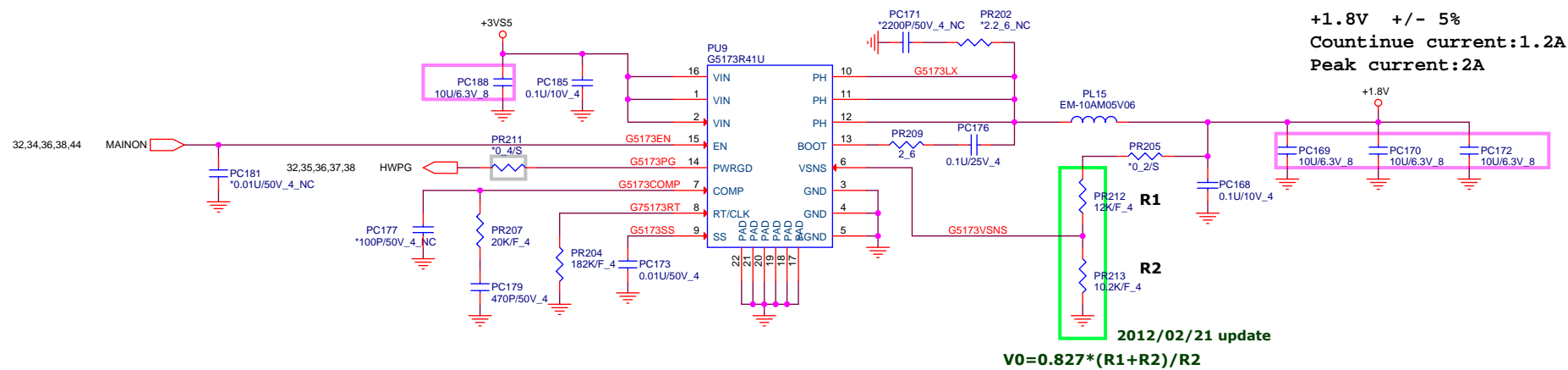
CPU	PR171
SV	100K/F_4
ULV	N.C



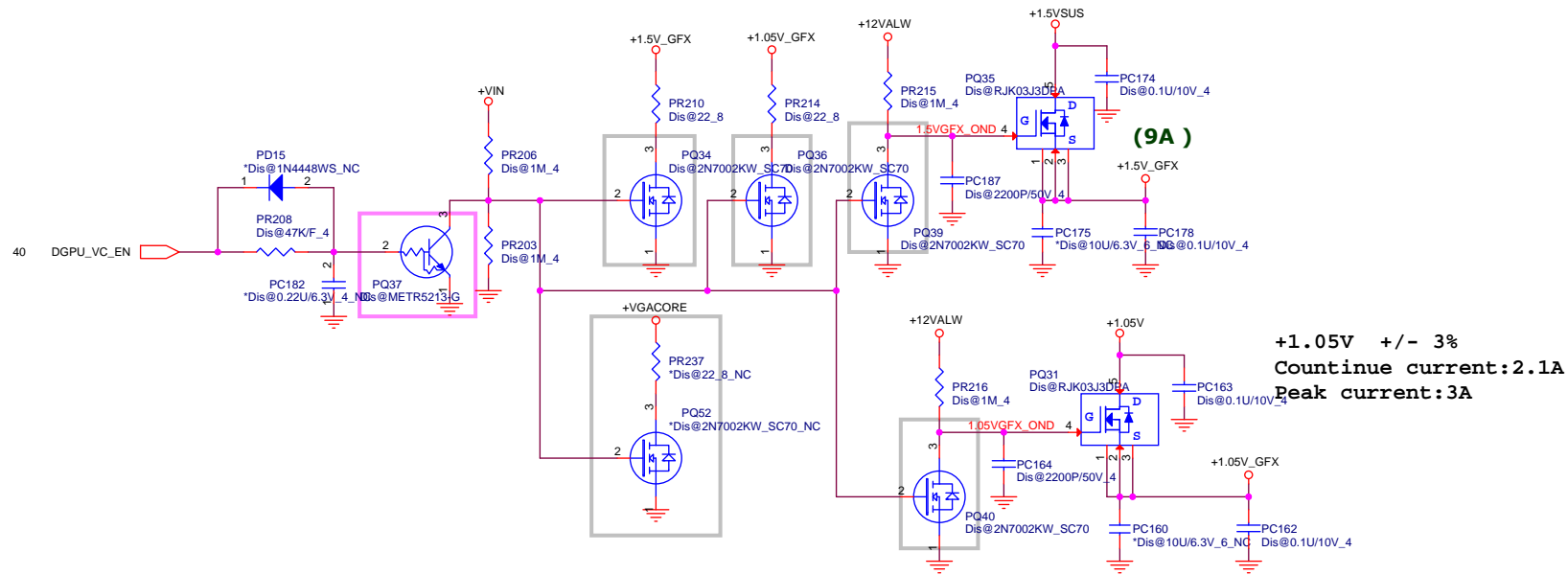
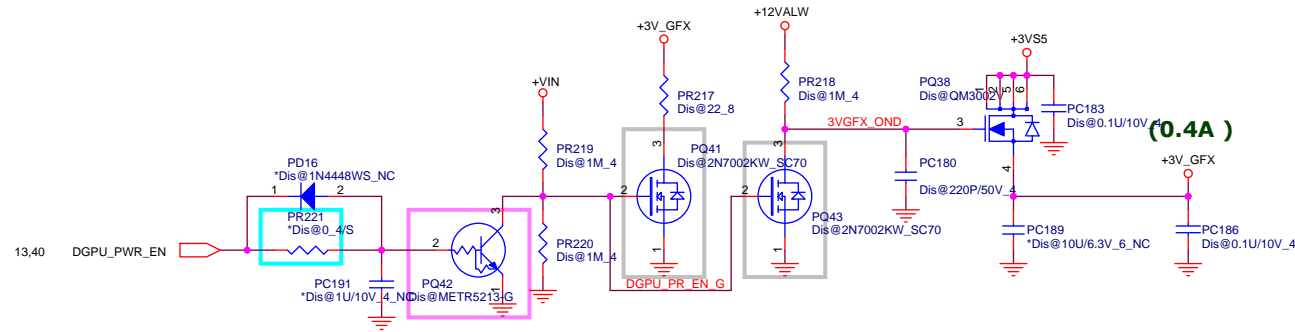
Quanta Computer Inc.
 PROJECT : JW8

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	+VCCSA (TPS51462RGER)	3A
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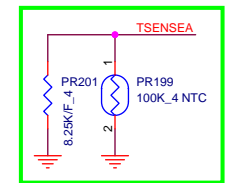
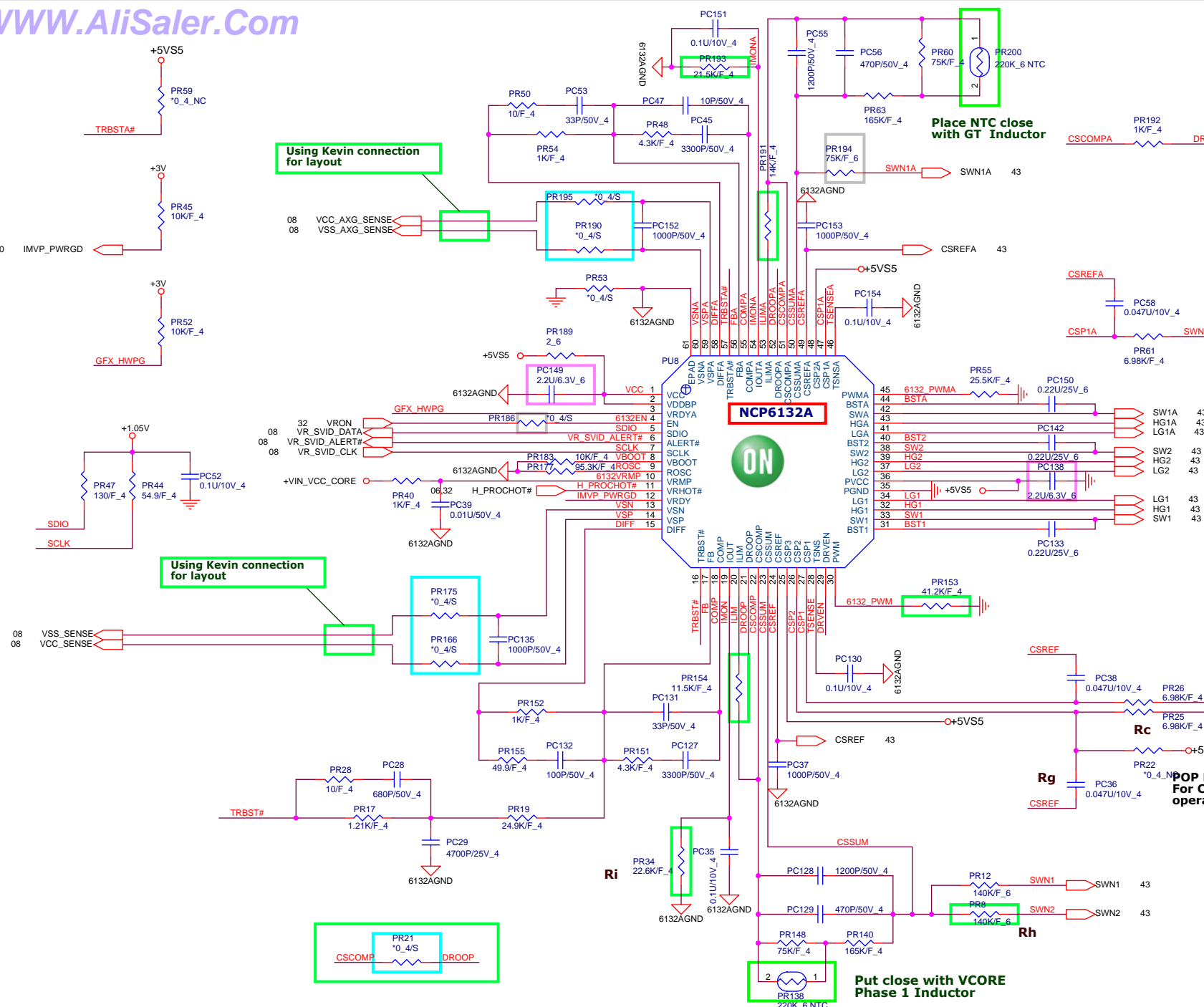


06,08,16,17,18,31,36 +1.5VSUS
10,11,12,13,14,25,29,30,31,32,33,35,38,39,44 +3VS5
19,21,22,40 +3V_GFX
20,21,22,23 +1.5V_GFX
19,20,21,31 +1.05V_GFX
44 +12VALW
06,08,10,11,12,14,25,32,37,38,42 +1.05V



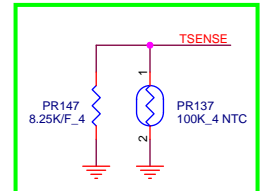
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	+VGA POWER	3A
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Place NTC close with V_GT hot spot

ULV Mode N.C
PR25, PC36, PC142, PR8



Place close with VCORE hot spot

+VCC_CORE (ULV 17W)

TDC : 25A

Peak current: 33A

Load Line : -2.9mV/A

Countinue current:33A

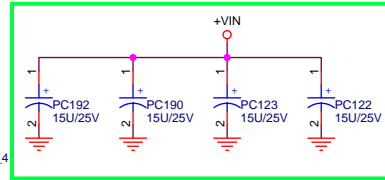
Peak current: 53A

Load Line : -1.9mV/A

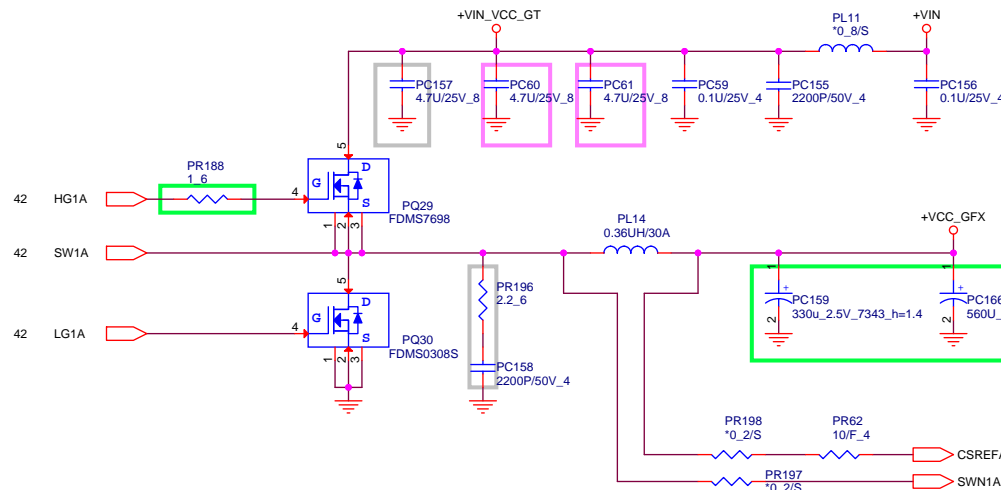
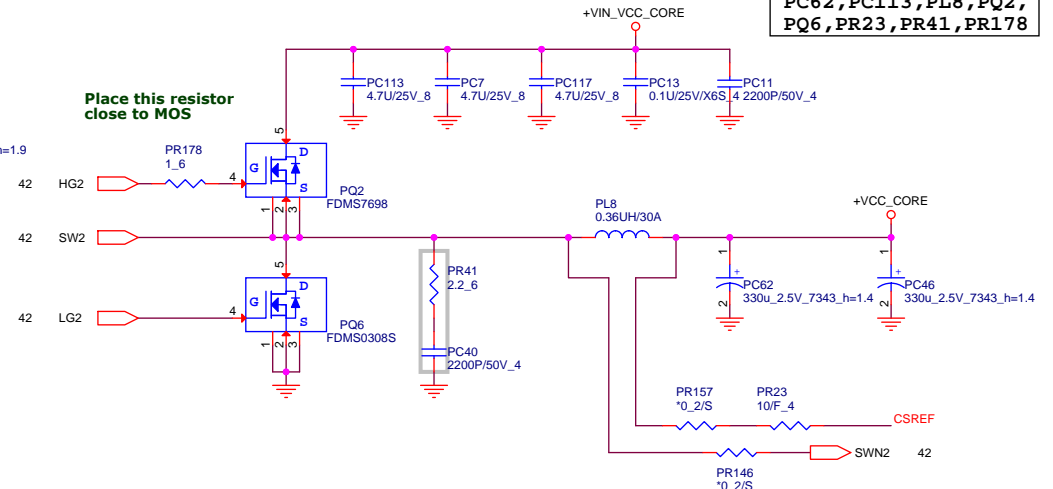
ULV Mode N.C

PC7,PC11,PC13,PC40,
PC62,PC113,PL8,PQ2,
PQ6,PR23,PR41,PR178

Place this resistor
close to MOS



Place this resistor
close to MOS



+VCC_GFX

Countinue current:21.5A

Peak current: 33A

Load Line : -3.9mV/A



Quanta Computer Inc.

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	CPU Core2 (NCP5911)DC	3A
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